MULTILEVEL POWER CONVERTERS FOR RENEWABLE ENERGY SOURCES AND ELECTRIC TRACTION COMBINING SILICON AND WBG DEVICES

A Thesis Submitted in Partial Fulfilment of the Requirements
for the Degree of Doctor of Philosophy in

Sustainable Development and Climate change

Doctoral Programme of National Interest

In the Curriculum
TECHNOLOGY AND TERRITORY

Gioele Baia

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IUSS
Scuola Universitaria Superiore Pavia

Università degli Studi di Messina

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PhD SDC
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AND CLIMATE CHANGE

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By

Gioele Baia

Supervisor: Prof. Antonio Testa

Co-Supervisor: Prof. Cedric Caruana Mifsud

ABSTRACT

The growing global demand for energy and the urgent need to reduce greenhouse gas emissions have accelerated the transition from fossil fuel-based systems toward cleaner and more efficient technologies. In the power generation sector, renewable energy sources such as solar and wind have become increasingly prominent; however, their intermittent nature poses significant challenges for stable and reliable grid integration. At the same time, the transportation sector is undergoing a similar transformation, with the shift from conventional internal combustion engines to electric mobility solutions aimed at achieving sustainable and low-emission transportation. In both stationary and mobile applications, power electronics play a critical role by enabling efficient energy conversion, control, and storage. Through advanced converters, inverters, and control strategies, power electronics ensure seamless interaction between renewable sources, energy storage systems, and electric drives, enhancing overall efficiency, reliability, and flexibility across the entire energy ecosystem.

Over the years, advancements in semiconductor technology have significantly improved the performance of power converters, progressively reducing cost, while increasing overall system efficiency. Silicon-based Insulated Gate Bipolar Transistors (Si-IGBTs) are widely utilized in renewable energy and e-mobility applications due to their capability to handle high voltages and currents with relatively low conduction losses. However, some intrinsic deficiencies of these devices have driven the development of devices based on wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC-MOSFET) and gallium nitride (GaN). These materials exhibit superior electrical and thermal properties, enabling higher switching frequencies, lower losses, and increased power density. Such advantages make WBG devices ideal for applications in renewable energy systems, electric traction, and industrial power conversion.

A widespread adoption of WBG semiconductors is expected to play a pivotal role in improving the performance of future generations of sustainable energy

systems and electric vehicles in the near future. However, the cost of these devices currently exceeds that of conventional Si-IGBTs by a significant margin. To speed up the introduction of WBG devices, this thesis investigate multilevel converter structures that combine Si-IGBTs and WBG devices to improve efficiency at a reasonable cost for use in electric vehicles, wind power, photovoltaic generators, and Flexible AC Transmission System (FACTS) applications.

This investigation integrates theoretical modeling, simulation, and experimental validation to evaluate the feasibility and effectiveness of the proposed approaches in real-world power conversion systems. Particular emphasis is placed on assessing the impact of the proposed approaches on efficiency, cost, energy savings, and thermal management.

The different types of power devices used in renewable energy and electric mobility applications (Si-IGBT, SiC-MOSFET, and GaN HEMTs), are first analyzed from a physical perspective, highlighting their advantages and disadvantages. Subsequently, the conducted studies and their application in the fields of energy generation from renewable sources and electric mobility will be presented, demonstrating the benefits in terms of energy efficiency and cost of the proposed approach in real-world power conversion systems.

ACKNOWLEDGEMENTS

This thesis is the result of the research conducted during my PhD at the Power Electronics Laboratory of the University of Messina. It focuses on simulation and experimental analysis of semiconductors, contributing to the laboratory's recent scientific production.

In this regard, I would like to express my gratitude to all the colleagues with whom I have collaborated, and specifically to my supervisor, Full Professor Antonio Testa, and Associate Professor Salvatore Foti.

Artificial Intelligence tools have been utilized in some sections to refine the linguistic style and improve readability.

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Introduction, classification and evolution of multilevel inverters.

1 INTRODUCTION, CLASSIFICATION AND EVOLUTION OF MULTILEVEL INVERTERS.

1.1 INTRODUCTION.

Since the 1990s, increasing awareness of air pollution and climate change has highlighted the urgent need to reduce greenhouse gas emissions, particularly carbon dioxide (CO_2), which is the primary contributor to global warming, as shown in fig.1.1 [1].

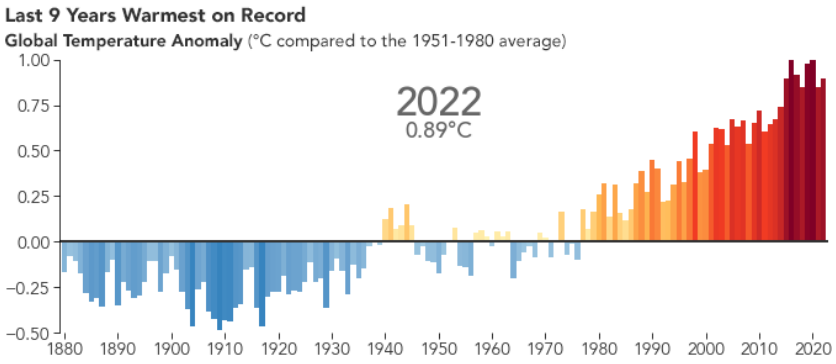


Fig. 1.1 Global emissions rising.

The concentration of atmospheric carbon dioxide (CO_2) has reached unprecedented levels, setting new records year after year [2]. The long-term increase in atmospheric CO_2 levels is primarily driven by human activities, particularly the combustion of fossil fuels such as coal, oil, and natural gas. These fuels contain carbon that was sequestered over millions of years through photosynthesis, but human industrial activity has been returning this stored carbon to the atmosphere at an accelerated pace. Although natural carbon sinks, such as forests and oceans, help absorb a portion of emitted CO_2, they can only remove about half of the carbon dioxide released into the atmosphere annually. As a result, CO_2 concentrations continue to rise beyond the rate at which natural processes can mitigate them. The more emissions exceed natural

absorption capacity, the faster the atmospheric concentration of CO_2 increases as shown in Fig. 1.2.

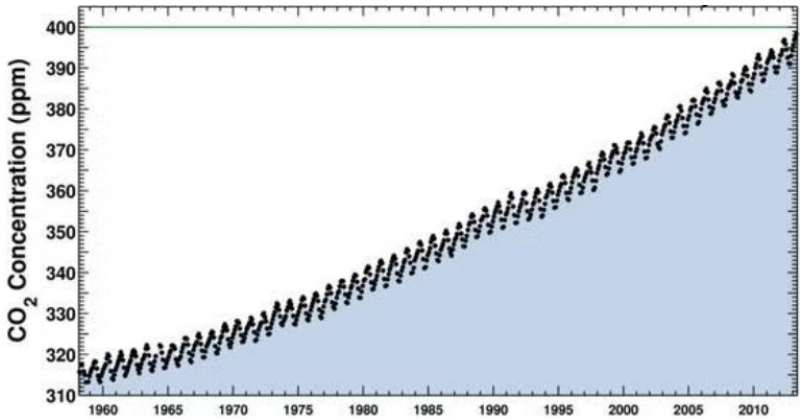


Fig. 1.2 CO2 Global emissions.

The decarbonization of the global economy presents a critical and multifaceted challenge. Achieving the emission reduction targets established by regulatory bodies requires the development of increasingly efficient electronic systems. For instance, projections indicate that global energy consumption will rise by approximately 40% by the year 2040 [3]. Notably, around 60% of this demand is expected to be met by electrical energy, where power converters will play a central role, particularly in the management and control of renewable energy sources integrated into the electrical grid. This trend will be driven by the rapid adoption of electric vehicles (EV), the expansion of green hydrogen production, and the continuous increase in installed capacity of renewable energy sources (RES). The emission can be either reduced or eliminated by hybrid or pure-electric transportation. Other than the reduction in gas emissions, transportation electrification leads to higher energy efficiency, better acceleration, and less required maintenance [4]. On the other hand, long charging time and low maximum driving range of battery-powered electric vehicles (BEV), trucks, and buses before recharging are still the biggest challenges which are impeding the fast growth of transportation electrification [5]. As a result, the performance, efficiency, and reliability of power electronic converters will become even more critical in enabling the transition to a sustainable energy infrastructure. In particular greenhouse gas emissions (GHG) of the transportation sector was 28% share of total emissions in the United States in 2018 [6]. In fig. 1.3 it can be seen that the transportation sector has been a major source of CO_2

emissions, leading to a strong push for the adoption of electric mobility as a more sustainable alternative to fossil fuel-powered vehicles.

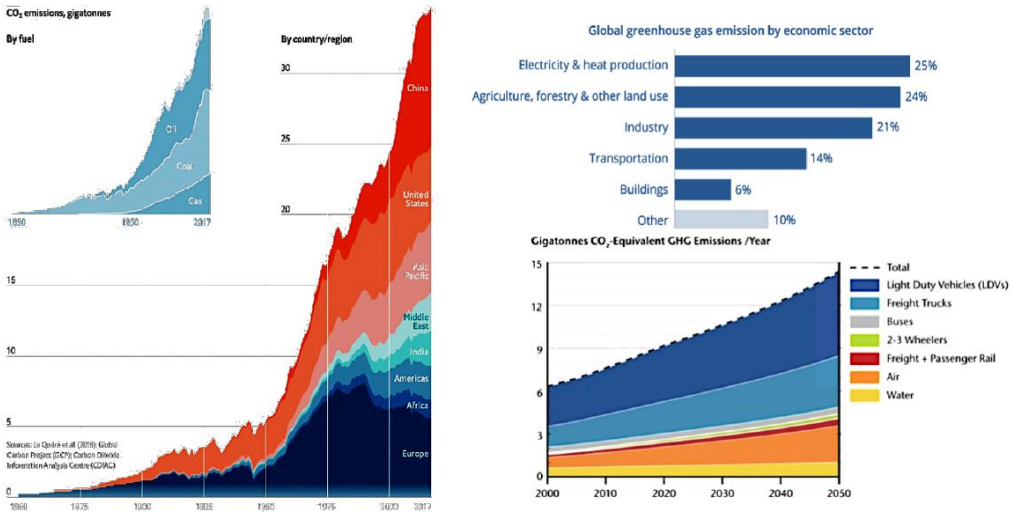


Fig. 1.3 Global emissions.

This rapid accumulation of greenhouse gases is a primary driver of global climate change, contributing to rising global temperatures, ocean acidification, and extreme weather patterns. A widespread transition to EV is considered essential for lowering fossil fuel demand and reducing emissions. However, the environmental benefits of EV depend not only on the decarbonization of the energy grid but also on the efficiency of the power conversion systems they rely on. More efficient power converters in EV can significantly reduce indirect emissions by lowering energy losses during charging and operation, ensuring that more of the electricity consumed is effectively utilized.

1.2 POWER CONVERTERS.

Power electronics has undergone significant advancements over the past decades, driven by the need for higher efficiency, improved power quality, and reduced environmental impact. This highlights the crucial role of power electronics in mitigating environmental impact, not only in transportation but also in renewable energy integration and industrial applications. The evolution of power semiconductor devices has played a crucial role in enabling the transition from conventional fossil fuel-based energy systems to more sustainable alternatives, including renewable energy integration and electric propulsion

systems. Power converters can be classified based on the waveforms of input and output electric quantities into the following categories:

- DC to DC converters, which convert one DC voltage level to another one and are commonly used in portable electronics such as laptops and mobile phones, as well as in electric vehicles and renewable energy systems [7];
- DC to AC converters (Inverters), which convert direct current to alternating current and are essential in solar and wind power systems, uninterruptible power supplies (UPS), and electric vehicles (EV) [8];
- AC to DC converters (Rectifier), which transform alternating current into direct current, finding applications in power supplies, battery chargers, and electric vehicle charging stations [9];
- AC to AC converters, which modify AC voltage or frequency, and are used in voltage regulators, motor speed control, and HVAC (heating, ventilation, and air conditioning) systems [10].

In the field of electric mobility, power converters are the backbone of powertrain systems, enabling efficient conversion of electrical energy from batteries to drive electric motors. Unlike traditional internal combustion engine (ICE) vehicles, which rely on mechanical transmissions, EVs utilize power electronics to regulate motor speed and torque. This regulation is made possible by inverters, which convert DC from high-voltage batteries into a controlled AC suitable for permanent magnet synchronous machines (PMSM) or induction motors (IM). The efficiency of this conversion process is paramount, as it directly influences the vehicle's range, performance, and overall energy consumption. High-efficiency inverters contribute to reducing thermal losses, improving battery utilization, and ultimately extending the driving range per charge. Figure 1.4 illustrates different power converter topologies, including voltage source converters (VSCs), current source converters (CSCs), and Z-source converters.

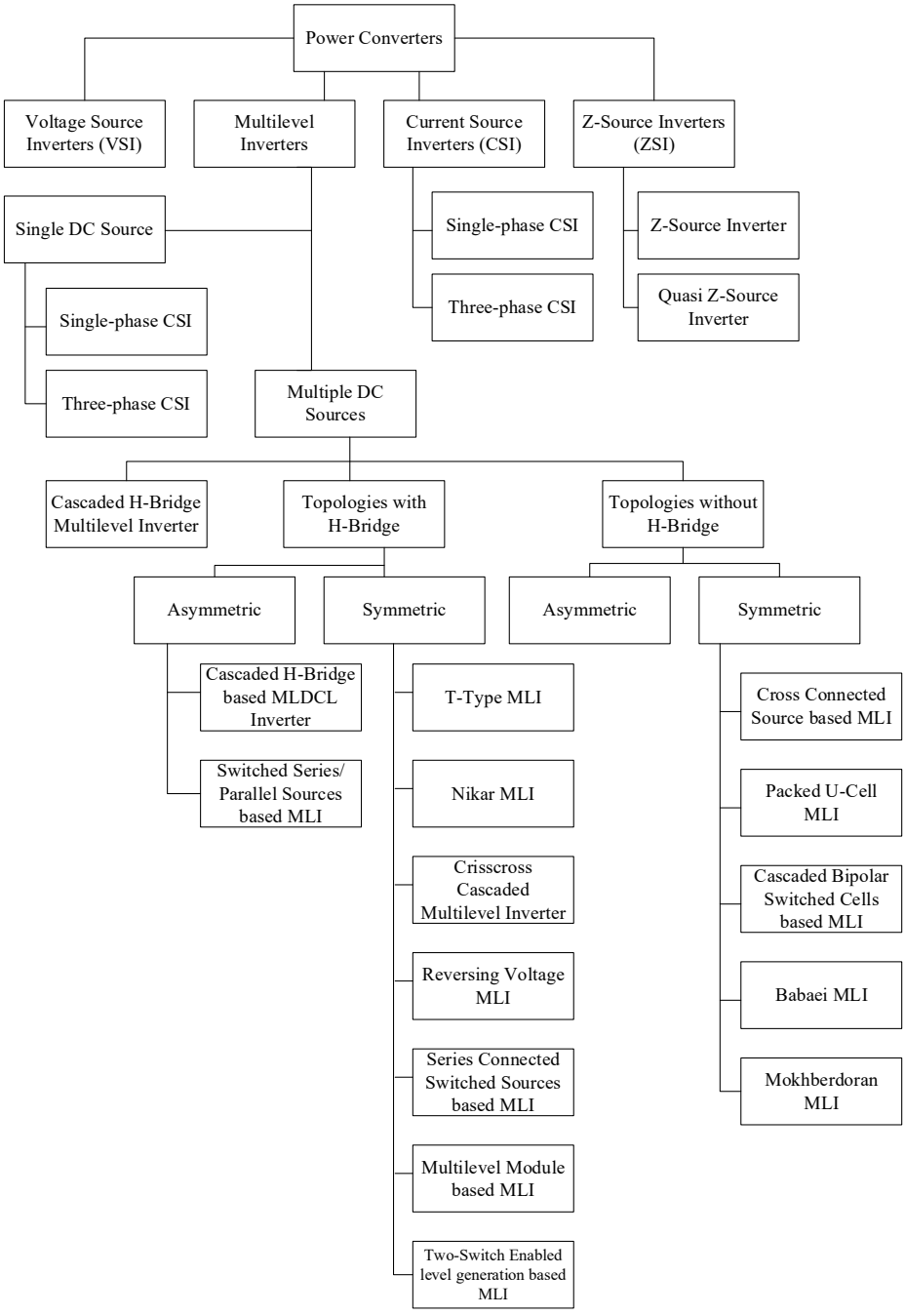


Fig. 1.4 Power converters topologies.

1.3 MULTILEVEL INVERTER TOPOLOGIES.

A three-phase two-level converter is a power electronic device that converts DC voltage into a three-phase AC output when operating as an inverter and conversely converts AC power into DC power when operating as a rectifier. It is widely used in applications such as motor drives, renewable energy systems, and power transmission. The inverter consists of three legs, each corresponding to one of the three output phases (A, B, and C). As shown in Fig.1.5, each leg contains two power switches (such as Si-IGBTs, Si-MOSFETs, or WBG devices like SiC or GaN), which alternately switch on and off to generate a quasi-sinusoidal waveform which approximates the desired AC voltage waveform. The quality of the voltage at the output terminals (V_{An}, V_{Bn}, V_{Cn}) depends on the DC bus voltage (V_{DC}) and the switching frequency, and ultimately on the characteristics of semiconductor devices. These semiconductor characteristics will be further analyzed in Chapter 2.

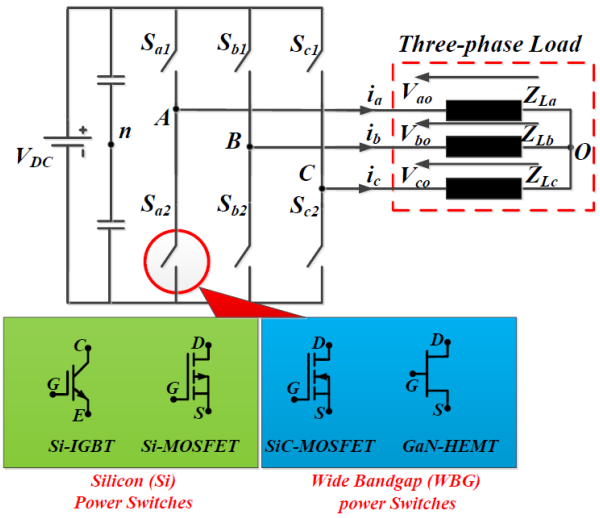


Fig. 1.5 Two level three-phase inverter.

Multilevel converters (MLC) were initially developed to overcome the limitations of conventional two-level inverters, particularly in terms of voltage stress on switching devices [11-17]. As shown in Fig.1.6, by connecting multiple power switches in series, the multilevel inverter (MLI) distributes the DC voltage across several components, thereby enhancing reliability and efficiency and reducing voltage stress on the devices. The introduction of multiple voltage levels also

reduces total harmonic distortion (THD), bringing the output waveform closer to an ideal sinusoidal shape and reducing electromagnetic interference (EMI). As the demand for higher efficiency, better power quality, and increased reliability continues to grow, research in advanced MLC topologies remains a pivotal area of innovation. The transition from two-level to multilevel converters represents a fundamental step toward achieving more sustainable, high-performance power conversion systems, both in energy transmission and electric mobility.

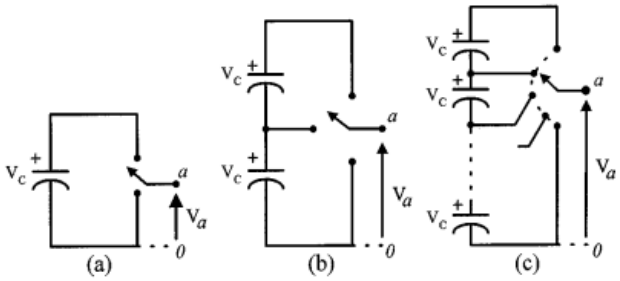


Fig. 1.6 Phase leg of an inverter: (a) two levels, (b) three levels, and (c) n-levels.

Multilevel converters can be classified into five main topologies:

- Neutral Point Clamped (NPC);
- Flying Capacitor (FC);
- Cascaded H-bridge (CHB);
- T-Type (TT);
- Modular Multilevel Converters (MMC).

Figure 1.7 shows the evolution of MLIs through recent past years.

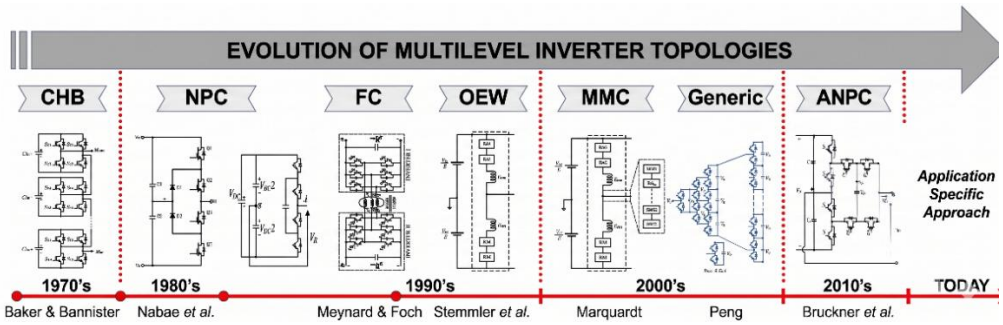


Fig. 1.7 Evolution of MLIs.

In general, multilevel inverter topologies offer:

- Reduced total harmonic distortion: By producing output voltage waveforms with multiple levels, MLIs achieve lower THD, thereby reducing filtering requirements and improving power quality [18];
- Reduction of common-mode voltage: which prevents degradation of motor bearings [19];
- Lower switching losses: The partition of the input voltage among multiple semiconductor devices allows for lower individual device stress, enabling operation at lower switching frequencies without compromising performance [20];
- Higher efficiency and reduced thermal stress: Lower voltage stress across switching devices results in reduced conduction and switching losses, improving overall system efficiency and reliability [21];
- Scalability for high-voltage applications: MLIs facilitate the use of lower-rated semiconductor devices, making them suitable for medium- and high-voltage applications without the need for bulky transformers [22].

Currently, MLIs are extensively employed in medium-voltage, high-power applications, particularly in variable-speed motor drives, including industrial motors, pumps and electric traction systems [23-24]. Additionally, MLCs play a crucial role in power conditioning applications such as voltage rectifiers, static compensators (STATCOM), and back-to-back inverters connected to power grids [25-26].

1.3.1 Neutral Point Clamped inverter.

The Neutral-Point-Clamped inverter was introduced in the 1980s as an extension of conventional two-level inverters, aimed at increasing voltage handling capability without requiring devices rated for the full DC bus voltage. This is achieved through the use of clamping diodes, which connect the intermediate points of the DC bus to the neutral node, thereby enabling multiple voltage levels at the output, as shown in Fig. 1.8.

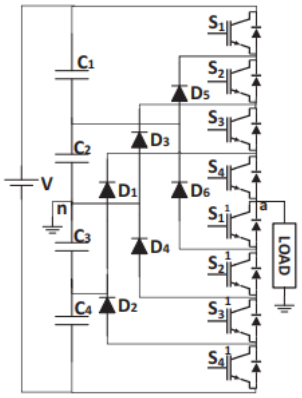


Fig. 1.8 NPC inverter.

In a three-level NPC inverter, the output voltage can take three distinct values: $+V_{DC/2}$, 0, and $-V_{DC/2}$. This topology halved the voltage stress on individual devices, effectively doubling the manageable operating voltage without necessitating precise voltage matching, making it a dominant solution in the 1980s [27]. The general expression for the output voltage in an N-level NPC inverter is:

$$V_{an} = \frac{kV_{DC}}{(n-1)} \tag{1}$$

where *k* can take values in the range $(-n+1, \dots, 0, \dots, n-1)$. One of the main challenges of the NPC topology is maintaining the balance of the neutral point voltage, as imbalances can cause undesired harmonic distortion and increased stress on semiconductor devices. Various modulation techniques, such as space vector modulation (SVM) and carrier-based pulse width modulation (PWM), have been developed to mitigate this issue.

1.3.2 Cascaded H-Bridge inverter.

The CHB topology was patented by Baker and Bannister in the 1970s [28], it can generate multilevel voltage using multiple independent DC sources, as shown in Fig. 1.9. This topology, known as cascaded inverter, connects full-bridge cells in series using separate DC sources to produce a staircase AC voltage. Despite being developed earlier, the cascaded inverter did not gain

widespread industrial adoption until the mid-1990s. Each H-bridge is powered by an independent DC source, which enables the synthesis of a stepped output voltage with multiple levels. The number of levels in the output voltage waveform is determined by the number of H-bridge modules, following the relationship $2n + 1$, where *n* is the number of H-bridge units per phase. The total output voltage of a CHB inverter is given by:

$$V_{out} = \sum_{i=1}^{n} V_i \tag{2}$$

where V_i is the output voltage of the *i*-th H-bridge module. CHB inverters offer superior scalability, modularity, and efficiency, making them well-suited for medium- and high-voltage applications such as electric drives and renewable energy systems. However, the requirement for multiple isolated DC sources can be a drawback, as it complicates the power supply architecture.

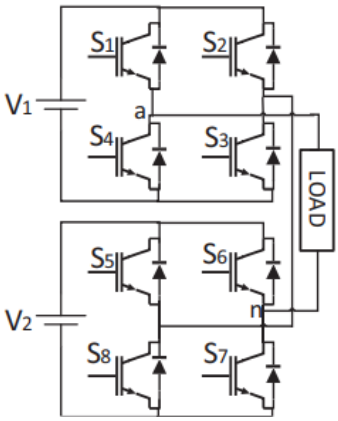


Fig. 1.9 CHB inverter.

1.3.3 T-Type inverter.

The T-Type Multilevel inverter is a variation of the Neutral-Point-Clamped inverter, designed to reduce switching losses and improve efficiency by eliminating the need for clamping diodes. Instead, it employs semiconductor switches to connect the midpoint of the DC bus to the neutral point, forming a distinctive "T" structure. This topology [29] was put forward in 2006 to alleviate

the drawbacks associated with TLI and NPC solutions while simplifying the circuit and enhancing efficiency and it is shown in fig. 1.10. The inverter operates by switching between different voltage states, typically producing three output voltage levels: $+V_{DC/2}$ (in case of the positive half cycle), 0 (in case neutral state is activated), and $-V_{DC/2}$ (in case of negative half cycle). The elimination of diodes leads to a reduction in conduction losses, making this topology attractive for applications requiring high efficiency and moderate power levels.

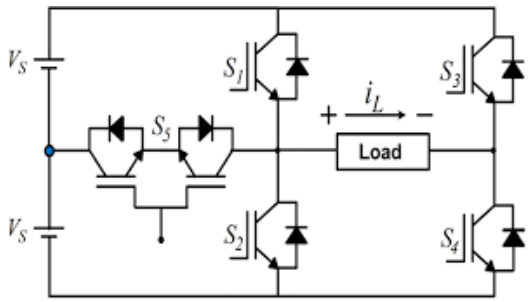


Fig. 1.10 - T-Type inverter.

1.3.4 Flying Capacitor inverter.

In the 1990s, Meynard and Foch introduced the FC inverter, which incorporates balancing capacitors, DC-link capacitors, and switching devices to regulate voltage levels [30]. Increasing the number of levels in an inverter enhances the output voltage waveform, resulting in a staircase approximation of a sinusoidal signal with reduced harmonic distortion. However, a greater number of levels also increases the complexity of control and introduces challenges such as voltage imbalance. This inverter operates on a principle similar to that of the NPC inverter, but instead of using clamping diodes, it employs additional capacitors to generate intermediate voltage levels, as shown in fig. 1.11. These capacitors are dynamically charged and discharged in a controlled manner to ensure the desired voltage levels at the inverter output. Like the NPC topology, the FC inverter can generate multiple voltage levels, but it offers the advantage of increased redundancy, as different switch combinations can produce the same output voltage. The governing equation for the output voltage of an FC inverter is

$$V_{an} = \sum_{i=1}^{m} Vc_i \tag{3}$$

where Vc_i represents the voltage across the *i*-th flying capacitor, and *m* is the number of capacitors. A significant challenge in this topology is maintaining the voltage balance of the flying capacitors, which requires sophisticated control strategies. The increased number of capacitors also adds complexity in terms of physical size and cost, making FC inverters less common in industrial applications compared to NPC or cascaded H-bridge inverters.

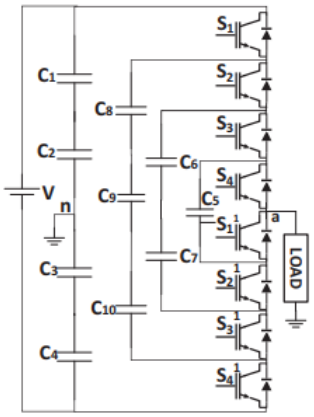


Fig. 1.11 FC inverter.

1.3.5 Modular Multilevel Converter.

The Modular Multilevel Converter topology is used in high-voltage direct current (HVDC) transmission and industrial applications requiring ultra-high-power levels. As shown in fig. 1.12, the MMC consists of multiple submodules per leg, with each submodule containing a capacitor and semiconductor switches that allow selective inclusion or exclusion of the submodule's capacitor in the output voltage generation. This topology enables fine-grained voltage control with an almost perfect sinusoidal waveform, eliminating the need for extensive filtering. The output voltage equation for an MMC is:

$$V_{out} = \sum_{i=1}^{N} Vc_i \qquad (4)$$

where Vc_i is the voltage of the *i*-th submodule capacitor, and N is the total number of submodules per phase leg. MMC inverters offer unparalleled efficiency, scalability, and harmonic performance. However, they require complex control algorithms to manage capacitor voltage balancing and ensure stable operation.

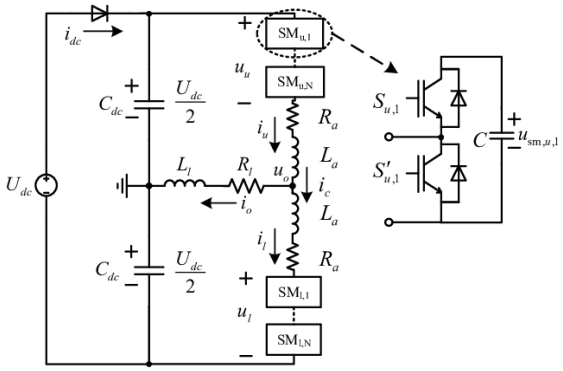


Fig. 1.12 MMC inverter.

1.3.6 Open-End Winding inverter.

Open-end winding (OEW) power conversion systems are characterized by the accessibility of both ends of the phase windings of an AC rotating machine or an AC transformer. Although structurally different from standard architectures, the OEW configuration is classified as a multilevel converter because it feeds the load from both ends, generating a differential phase voltage with multiple steps that replicates the behavior and advantages of traditional multilevel inverters. The topology is shown in fig. 1.13.

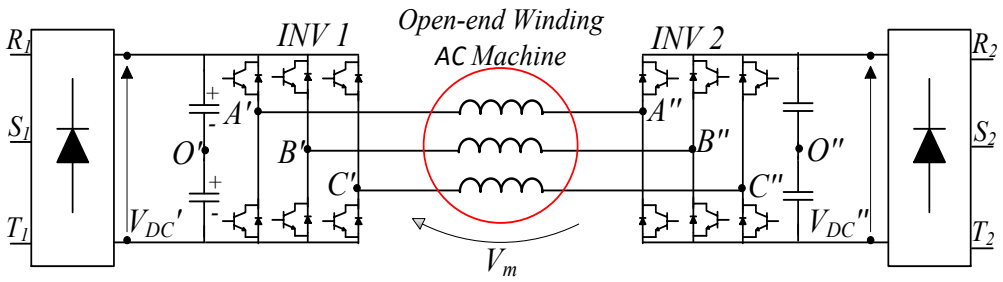


Fig. 1.13 OEW inverter.

One of the primary motivations for adopting OEW configurations is their ability to synthesize higher voltage levels at the terminals of an AC machine by using two two-level VSC. In comparison to two-level VSCs with star or delta connections, OEW configurations own the following advantageous features:

- The two converters can be configured to reduce the voltage rating of power switches, or to step up the converter output voltage rating;
- A fully independent control of the phase currents is possible;
- The frequency of the phase current ripple is equal to the sum of the switching frequencies of the two converters;
- A lower Common Mode Voltage (CMV) is achieved;
- A greater redundancy is achieved, which can be exploited to reconfigure the inverter in case of faults.

In addition to these advantages, being a multilevel configuration, it also inherits all the benefits previously described for a MLC. Carrier-based and SVPWM techniques have been employed to effectively manage these configurations, ensuring optimal performance [31]. Despite their advantages, implementing OEW systems presents specific challenges, particularly concerning the management of zero-sequence currents. In configurations featuring a common DC bus, pathways for zero-sequence currents can emerge, which, if not properly controlled, may compromise system performance. Advanced control strategies have been proposed to suppress these currents, ensuring stable and reliable operation. The integration of OEW systems into electric transportation [32-34] and in renewable energy systems [35-36] has been a focal point of recent research.

OEW power conversion systems have gained significant attention due to their ability to enhance efficiency, improve voltage control, and provide fault tolerance in various applications, including electric mobility and renewable energy integration. The development of advanced control strategies plays a critical role in maximizing the potential benefits of these systems while mitigating challenges such as zero-sequence currents, voltage imbalances, and harmonic distortions [37].

One of the key advantages of OEW inverters is their ability to generate multilevel voltage waveforms without the need for bulky passive filters. Various modulation strategies have been developed to optimize their performance:

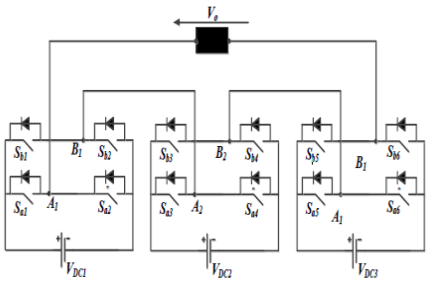
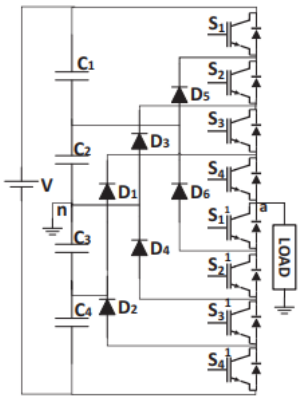
- Space Vector Pulse Width Modulation: This technique extends conventional SVPWM by considering the additional degrees of freedom provided by the open-end configuration, leading to improved harmonic performance and reduced switching losses [38].
- Carrier-Based PWM: Carrier phase-shifted and level-shifted PWM techniques have been explored to enhance power quality and minimize common-mode voltage [39].
- Selective Harmonic Elimination (SHE): A more sophisticated approach, SHE aims to eliminate specific lower-order harmonics, thus reducing the need for external filtering components [40]

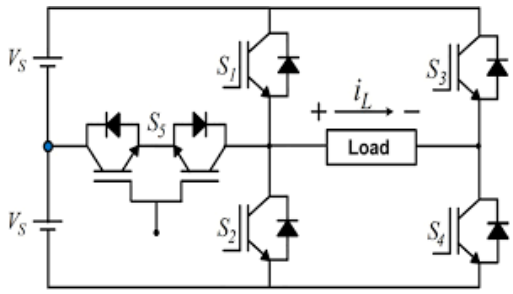
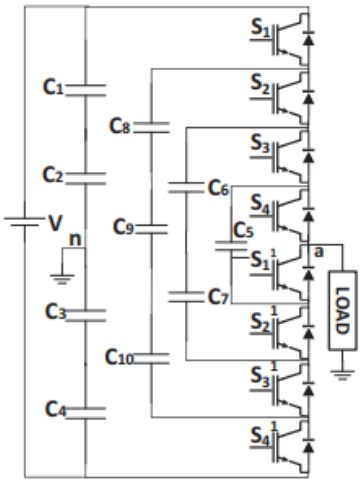
OEW inverters may also be utilized in numerous contexts:

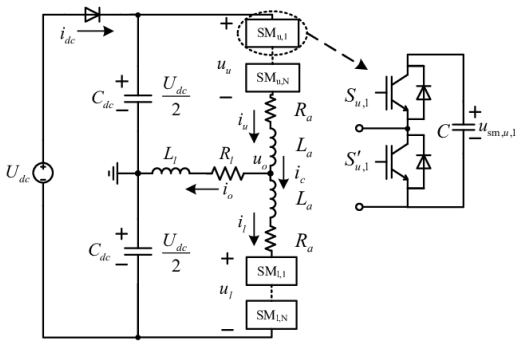
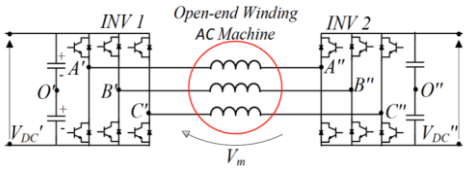
- Electric Vehicles: OEW inverters are used to drive PMSMs with enhanced torque ripple suppression and bidirectional energy flow for vehicle-to-grid (V2G) applications [41].
- Wind Energy Systems: OEW generators provide improved stability in variable-speed wind turbine applications [42].
- Grid-Connected Converters: OEW-based converters help integrate distributed renewable energy sources with enhanced fault ride-through (FRT) capabilities and improved power quality [43].

Table 1.1 shows advantages and limitations of MLIs.

Table 1.1 Different inverter topologies.

Topology	Advantages	Limitations
CHB **(Cascaded H-Bridge Inverter)** 	High reliability; Modular; No floating capacitors; Simple control.	Isolated DC power sources are required, which make grid-connected applications expensive; High number of power switches.
NPC - (Neutral Point Clamped) 	Good dynamic response; Simple design; Low cost and compact 3-L structure.	Unbalanced capacitor voltages; Increased cost and reduced reliability as the number of levels increase; Unequal loss in switches.

T-TYPE 	No additional diodes; No floating capacitors; Simple control.	Higher voltage stress on switches; Low efficiency at high frequency operation due to high switching losses; No suitable for high voltage, high power applications.
FC (Flying – Capacitor) 	Cost efficiency in higher level structures.	High number of floating capacitors; Complex control; High voltage ripple at low frequencies; Bulky and heavy; Requires plenty of voltage sensors; Low reliability.

MMC (Modular Multilevel Converter) 	High reliability; Modular; Scalable.	Large number of capacitors; Complex control; Pre-charging capacitor circuits; High voltage ripple at low frequency; Bulky and heavy; Requires lots of voltage sensors.
OEW (Open End Winding) 	Higher output voltage capability; Lower Harmonic Distortion (THD); Reduced common mode current.	More complex control and synchronization; Circulating currents between inverters; Higher cost and system complexity.

1.4 REFERENCE LIST.

[1] Hansen, J., R. Ruedy, M. Sato, and K. Lo (2010), Global surface temperature change, Rev. Geophys., 48, RG4004, doi:10.1029/2010RG000345;

[2] https://www.climate.gov/news-features/understanding-climate/climate-change-atmospheric-carbon-dioxide;

[3] F. Roccaforte, P. Fiorenza, G. Greco, R. Lo Nigro, F. Giannazzo, F. Iucolano, and M. Saggio, “Emerging trends in wide band gap semiconductors (SiC and GaN) technology for power devices,” Microelectronic Engineering, vol. 187-188, pp. 66–77, 2 2018;

[4] A. Adib et al., “E-mobility - advancements and challenges,” IEEE Access, vol. 7, pp. 165226–165 240, 2019;

[5] A. Tomaszewska et al., “Lithium-ion battery fast charging: A review,” eTransp., vol. 1, 2019, Art. no. 100011;

[6] “Sources of greenhouse gas emissions.” 2019. Available: https://www.epa.gov/ghgemissions/sources-greenhouse-gasemissions;

[7] S. A. Gorji, H. G. Sahebi, M. Ektesabi and A. B. Rad, "Topologies and Control Schemes of Bidirectional DC–DC Power Converters: An Overview," in *IEEE Access*, vol. 7, pp. 117997-118019, 2019, doi: 10.1109/ACCESS.2019.2937239.

[8] Sayed, Khairy, Abdulaziz Almutairi, Naif Albagami, Omar Alrumayh, Ahmed G. Abo-Khalil, and Hedra Saleeb. 2022. "A Review of DC-AC Converters for Electric Vehicle Applications" *Energies* 15, no. 3: 1241. https://doi.org/10.3390/en15031241

[9] S. Roy, A. N. M. W. Azad, S. Baidya and F. Khan, "A Comprehensive Review on Rectifiers, Linear Regulators, and Switched-Mode Power Processing Techniques for Biomedical Sensors and Implants Utilizing in-Body Energy Harvesting and External Power Delivery," in *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12721-12745, Nov. 2021, doi: 10.1109/TPEL.2021.3075245.

[10] J. W. Kolar, T. Friedli, J. Rodriguez and P. W. Wheeler, "Review of Three-Phase PWM AC–AC Converter Topologies," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 11, pp. 4988-5006, Nov. 2011, doi: 10.1109/TIE.2011.2159353.

[11] S. Munawar, M. S. Iqbal, M. Adnan, M. Ali Akbar and A. Bermak, "Multilevel Inverters Design, Topologies, and Applications: Research Issues, Current, and Future Directions," in IEEE Access, vol. 12, pp. 149320-149350, 2024, doi: 10.1109/ACCESS.2024.3472752;

[12] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, Aug. 2002, doi: 10.1109/TIE.2002.801052;

[13] Rehaoulia, Abir & Rehaoulia, Habib & Fnaiech, Farhat. (2016). Multilevel Inverters Power Topologies and Voltage Quality: A Literature Review. Journal of Magnetics. 21. 83-93. 10.4283/JMAG.2016.21.1.083;

[14] A. R. Adly, H. Y. Abdul-Hamid, A. Elhussiny, M. S. Zaky and E. E. El-Kholy, "A Brief Review of the Conventional and Multilevel Inverters Topologies," 2023 IEEE Conference on Power Electronics and Renewable Energy (CPERE), Luxor, Egypt, 2023, pp. 1-8, doi: 10.1109/CPERE56564.2023.10119633;

[15] Peeyush Kala, Sudha Arora, A comprehensive study of classical and hybrid multilevel inverter topologies for renewable energy applications, Renewable and Sustainable

Energy Reviews, Volume 76, 2017, Pages 905-931, ISSN 1364-0321, https://doi.org/10.1016/j.rser.2017.02.008;

[16] A. El-Hosainy, H. A. Hamed, H. Z. Azazi and E. E. El-Kholy, "A review of multilevel inverter topologies, control techniques, and applications," 2017 Nineteenth International Middle East Power Systems Conference (MEPCON), Cairo, Egypt, 2017, pp. 1265-1275, doi: 10.1109/MEPCON.2017.8301344.

[17] A. Poorfakhraei, M. Narimani and A. Emadi, "A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends," in IEEE Open Journal of Power Electronics, vol. 2, pp. 155-170, 2021, doi: 10.1109/OJPEL.2021.3063550;

[18] S. Maurya, D. Mishra, K. Singh, A. K. Mishra and Y. Pandey, "An Efficient Technique to reduce Total Harmonics Distortion in Cascaded H- Bridge Multilevel Inverter," 2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), Coimbatore, India, 2019, pp. 1-5, doi: 10.1109/ICECCT.2019.8869424;

[19] Turzyński M, Musznicki P. A Review of Reduction Methods of Impact of Common-Mode Voltage on Electric Drives. Energies. 2021; 14(13):4003. https://doi.org/10.3390/en14134003;

[20] A. Singh, V. Jately, P. Kala, Y. Yang and B. Azzopardi, "Advancements in Multilevel Inverters for Efficient Harnessing of Renewable Energy: A Comprehensive Review and Application Analysis," in IEEE Access, vol. 12, pp. 156939-156964, 2024, doi: 10.1109/ACCESS.2024.3477501;

[21] S. M. Kim, E. J. Lee, J. S. Lee and K. B. Lee, "An Improved Phase-Shifted DPWM Method for Reducing Switching Loss and Thermal Balancing in Cascaded H-Bridge Multilevel Inverter," in IEEE Access, vol. 8, pp. 187072-187083, 2020, doi: 10.1109/ACCESS.2020.303026;

[22] S. Milovanovic and D. Dujic, "On Power Scalability of Modular Multilevel Converters: Increasing Current Ratings Through Branch Paralleling," in IEEE Power Electronics Magazine, vol. 7, no. 2, pp. 53-63, June 2020, doi: 10.1109/MPEL.2020.2984350;

[23] M. Carpita, M. Marchesoni, M. Pellerin and D. Moser, "Multilevel Converter for Traction Applications: Small-Scale Prototype Tests Results," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 2203-2212, May 2008, doi: 10.1109/TIE.2008.918645.

[24] S. Dieckerhoff, S. Bernet and D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," in *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1328-1336, Nov. 2005, doi: 10.1109/TPEL.2005.857534.

[25] W. Song and A. Q. Huang, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010, doi: 10.1109/TIE.2009.2036019.

[26] R. C. Portillo *et al*., "Modeling Strategy for Back-to-Back Three-Level Converters Applied to High-Power Wind Turbines," in *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1483-1491, Oct. 2006, doi: 10.1109/TIE.2006.882025

[27] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point-clamped PWM inverter", IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518-523, Sep. 1981;

[28] Baker, R.H. and Bannister, L.H. (1975) Electric Power Converter. US Patent US 386743A;

[29] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, 'A New Simplified Multilevel Inverter Topology for DC–AC Conversion', IEEE Trans. Power Electron., vol. 21, no. 5, pp. 1311–1319, 2006, doi: 10.1109/TPEL.2006.880303;

[30] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters", Proc. PESC Rec. 23rd Annu. IEEE Power Electron. Spec. Conf., pp. 397-403, Jun. 1992;

[31] E. Levi, N. Bodo, O. Dordevic and M. Jones, "Recent advances in power electronic converter control for multiphase drive systems," 2013 IEEE Workshop on Electrical Machines Design, Control and Diagnosis (WEMDCD), Paris, France, 2013, pp. 158-167, doi: 10.1109/WEMDCD.2013.6525176;

[32] Y. -F. Jia et al., "Control Strategy for an Open-End Winding Induction Motor Drive System for Dual-Power Electric Vehicles," in IEEE Access, vol. 8, pp. 8844-8860, 2020, doi: 10.1109/ACCESS.2020.2964105;

[33] D. De Simone, M. S. Carmeli, S. D'Arco, L. Piegari and P. Tricoli, "Design and Control of Hybrid Electric Light Rail Vehicles With Open Ended Winding Machines," in IEEE Open Journal of Vehicular Technology, vol. 5, pp. 695-703, 2024, doi: 10.1109/OJVT.2024.3400607;

[34] U. R. Muduli, A. R. Beig, K. Al Jaafari, J. Y. Alsawalhi and R. K. Behera, "An Improved Direct Torque Control with Battery Power Management of Open-End Winding Induction Motor Drive for Electric Vehicles," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 6332-6337, doi: 10.1109/ECCE44975.2020.9236199;

[35] Z. Zhang, X. Wang, J. Shen, S. Ren, D. Ma and D. Xiao, "Research on the Application of Open-End Winding PMSM in Renewable Energy System," 2023 26th International Conference on Electrical Machines and Systems (ICEMS), Zhuhai, China, 2023, pp. 3496-3500, doi: 10.1109/ICEMS59686.2023.10345000;

[36] R. Karampuri, S. Jain and V. T. Somasekhar, "A single-stage solar PV power fed Open-End Winding Induction Motor pump drive with MPPT," 2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Mumbai, India, 2014, pp. 1-6, doi: 10.1109/PEDES.2014.7041977;

[37] K. Safsouf, J. Sawma and H. Y. Kanaan, "A Comparative Study of Open-End Winding Drive Systems for Hybrid Fuel Cell-Battery Fed Electric Vehicles," 2021 IEEE 3rd International Multidisciplinary Conference on Engineering Technology (IMCET), Beirut, Lebanon, 2021, pp. 49-54, doi: 10.1109/IMCET53404.2021.9665621;

[38] F. F. V. Matos, H. O. Ramos, C. E. Oliveira, V. F. Mendes, M. A. S. Mendes and T. Meynard, "A vector modulation strategy for open-end winding conversion systems," 2018 IEEE International Conference on Industrial Technology (ICIT), Lyon, France, 2018, pp. 617-622, doi: 10.1109/ICIT.2018.8352249;

[39] P. Sandulescu, F. Meinguet, X. Kestelyn, E. Semail and A. Bruyère, "Control Strategies for Open-End Winding Drives Operating in the Flux-Weakening Region," in IEEE Transactions on Power Electronics, vol. 29, no. 9, pp. 4829-4842, Sept. 2014, doi: 10.1109/TPEL.2013.2283107;

[40] J. Riedemann, R. Peña, R. Cárdenas, J. Clare, P. Wheeler and R. Blasco-Gimenez, "Control strategy of a dual-inverter system for an open-end winding induction machine based on indirect matrix converter," 2014 16th European Conference on Power

Electronics and Applications, Lappeenranta, Finland, 2014, pp. 1-8, doi: 10.1109/EPE.2014.6910997;

[41] S. Foti, G. Baia, D. Campagna, H. Hassan Khan, A. Testa and S. De Caro, "Design and Development of a Mixed Si-GaN Open-End Winding Inverter for Electric Vehicles," in *IEEE Transactions on Transportation Electrification*, vol. 12, no. 1, pp. 1942-1954, Feb. 2026, doi: 10.1109/TTE.2025.3636205;

[42] Salvatore Foti, Antonio Testa, Gioele Baia, Haseeb Hassan Khan, Danilo Campagna, "A high efficiency three-port power converter for wind generators with energy storage, Journal of Energy Storage," Volume 116, 2025, 116029, ISSN 2352-152X, https://doi.org/10.1016/j.est.2025.116029;

[43] Salvatore Foti, Gioele Baia, Haseeb Hassan Khan, Antonio Testa, Michele Emanuele, "A T-STATCOM converter structure synergistically combining IGBTs and SiC-MOSFETs," Electric Power Systems Research, Volume 255, 2026, 112835, ISSN 0378-7796, https://doi.org/10.1016/j.epsr.2026.112835.

CHAPTER 2

Classification and evolution of semiconductor devices.

2 CLASSIFICATION AND EVOLUTION OF SEMICONDUCTOR DEVICES.

2.1 SEMICONDUCTORS.

Concerning the semiconductor devices employed within the inverters, a dedicated, in-depth analysis is warranted. As a cornerstone of power electronics, advancements in power semiconductor devices and semiconductor technology have played a pivotal role in he evolution and expansion of the entire power electronics industry, as illustrated in Fig. 2.1.

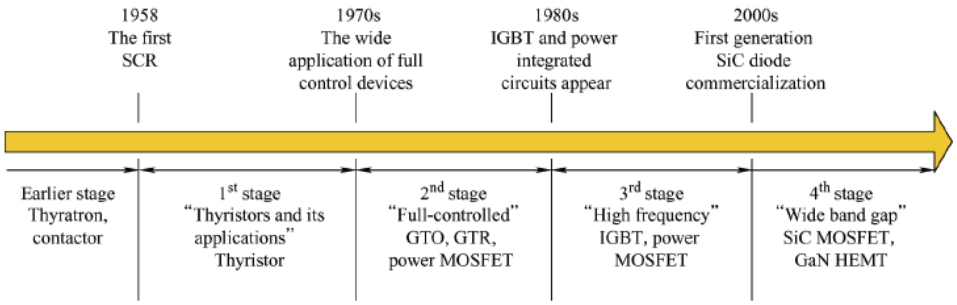


Figure 2.1 Development of semiconductor power devices.

Their technological evolution over time has been pivotal to the advancement of power conversion systems. Furthermore, a comprehensive comparison of these devices is essential to fully understand the specific advantages and disadvantages associated with adopting a particular technology for a given target application. In the early stages, germanium was the primary material used for semiconductor devices [1]. However, silicon quickly emerged as the dominant material due to its superior electrical and thermal properties, and it remains the industry standard to this day. Over time, advancements in fabrication technology have enabled the development of increasingly optimized and efficient electronic devices. In fact, since the invention of the thyristor in the 1950s, silicon-based semiconductor devices have dominated the field of power electronics due to the abundance of Si material, low production costs, and relatively simple manufacturing processes [2]. In the mid-1970s, the emergence and application of fully controllable devices, such as the gate turn-off thyristor (GTO), giant transistor (GTR), and power MOSFET, marked a significant

technological advancement, ushering in a new era for power electronics. The 1980s witnessed the introduction of MOS-controlled SI-IGBT devices and the commercialization of the power MOSFET, which catalyzed further development in power semiconductors and expanded their applications across various sectors. While MOSFETs offer clear advantages in high-frequency applications, their on-state resistance increases sharply with the blocking voltage, limiting their use primarily to medium- and low-voltage applications. In contrast, SI-Si-IGBTs, characterized by their low conduction losses and fast switching capabilities, are widely deployed in medium-frequency and high-power applications. [3-6]. In recent years, the integration of WBG devices, such as SiC and GaN [7-8] has enabled significant advancements in power converters originally based on Si devices, offering higher junction operating temperatures and faster switching capabilities [9]. The following are the key requirements for a controlled switch in power conversion applications:

- High blocking voltage capability when the switch is in the off-state.
- Low power dissipation to ensure high power conversion efficiency.
- High switching frequency to reduce the size and cost of passive components such as inductors and transformers.
- Normally-off operation, meaning the switch remains off when no control signal is applied and turns on only in response to a positive gate voltage.

A key concept in semiconductor physics is the bandgap energy (E_g), which represents the energy difference between the valence band and the conduction band of a material. For reference, metals have $E_g \approx 0eV$, while insulators may have $E_g \approx 4eV$ or higher. A larger bandgap allows for a thinner semiconductor substrate to withstand the same applied voltage, which is a fundamental advantage of WBG materials such as GaN and SiC. Drift velocity (v_s) defines the maximum speed at which charge carriers can move through a semiconductor. Higher drift velocity enables devices to operate at higher frequencies with lower switching losses, which is critical for modern high-efficiency power electronics. Another important aspect is the thermal conductivity, that refers to a material's ability to transfer heat through microscopic particle collisions and electron motion. Materials with high thermal conductivity can support higher operating temperatures, enhancing both reliability and power density. The overall performance of semiconductor devices

is also significantly influenced by differences in device structure and gate configurations. These parameters vary from one device to another and play a crucial role in determining switching behavior, voltage handling, and thermal performance [10].

2.1.1 Si-IGBTs.

Insulated Gate Bipolar Transistors (Si-IGBTs) are in high demand across critical applications such as wind energy systems, high-speed rail networks, and hybrid electric vehicles, all of which require power semiconductor devices capable of operating over a wide voltage range, from approximately *300V* to *6.5kV*. Si-IGBTs are based on silicon, which has a diamond cubic lattice structure held together by covalent bonds. This structure limits their electrical breakdown strength, as silicon's weak covalent bonds cannot withstand high electric fields. Silicon also has moderate carrier mobility and low thermal conductivity, leading to increased heat accumulation at high power levels. As a power semiconductor switch, the dynamic characteristics of the Si-IGBT receive particular attention. Its structure is shown in Fig. 2.2. In many applications, Si-IGBT dies are co-packaged with freewheeling diode dies, particularly in voltage source converters.

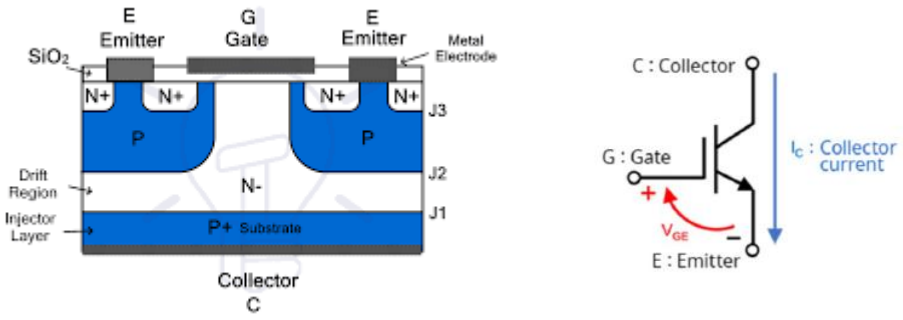


Fig. 2.2 Vertical Si-IGBT structure.

Due to its fast-switching behavior, the influence of parasitic circuit elements, such as stray inductances, on the Si-IGBT's electrical response becomes significant. Additionally, the gate drive circuitry plays a critical role in shaping the device's switching performance.

Figure 2.3 deals with a typical Si-IGBT turn-on and turn-off.

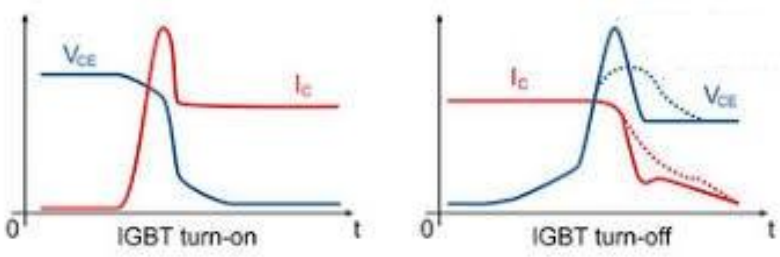


Figure 2.3 Si-IGBT turn-on and turn-off.

A characteristic phenomenon of the Si-IGBT in the well-known tail current during the final phase of the turn-off process, caused by excess carriers in the base recombining slowly. As a result, Si-IGBTs are burdened by relevant switching losses, which limit their efficiency in high-frequency applications. Consequently, their switching frequency typically ranges from *5kHz* to *50kHz*. Si-IGBTs are typically co-packaged with an anti-parallel freewheeling diode, which introduces a reverse recovery charge (Q_{RR}) that further contributes to switching losses. It also represents today a very cost-effective solution due to their mature manufacturing process, high production yields, and established supply chains, therefore, they dominate on application fields where cost and high voltage handling are the primary concerns.

2.1.2 SiC-MOSFET.

Although silicon (Si) has historically been the dominant material for power devices, Si-based technologies are now approaching fundamental limitations in terms of further performance enhancement. WBG semiconductors such as SiC and GaN have attracted growing interest as promising candidates for next-generation power electronics [11-13]. One of the fundamental advantages of silicon carbide as a semiconductor material lies in the significantly stronger atomic bonds compared to those in silicon. This characteristic is commonly expressed in terms of the material's wider energy bandgap, which ranges from *3.2eV* to *3.4eV* for SiC, in contrast to *1.12eV* for silicon. The wider bandgap underpins many of SiC superior electrical and thermal properties, including higher breakdown voltage, greater thermal conductivity, and improved high-

temperature performance. Another key advantage of this material is its significantly higher critical electric field strength, approximately ten times greater than that of Si. This allows for the design of voltage-blocking layers that are nearly ten times thinner and can support donor concentrations up to 100 times higher at the same breakdown voltage, compared to Si-based devices. Consequently, the theoretical unipolar limits of SiC devices are around 500 times lower than those of Si, as illustrated in Fig. 2.4. These superior material properties enable the development of highly efficient, compact, and thermally robust power devices, making SiC central to the advancement of modern power conversion systems [14].

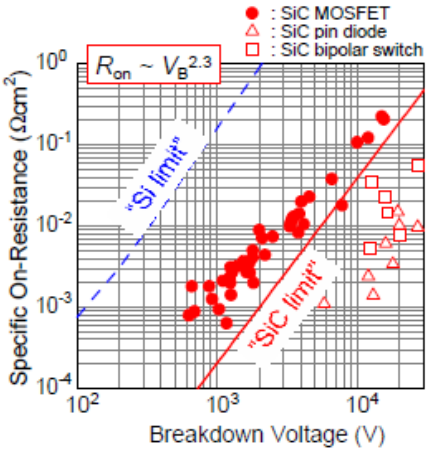


Figure 2.4 Trade-off between the on-resistance and breakdown voltage for Si and SiC unipolar devices.

The typical vertical structure of a SiC MOSFET is shown in fig. 2.5.

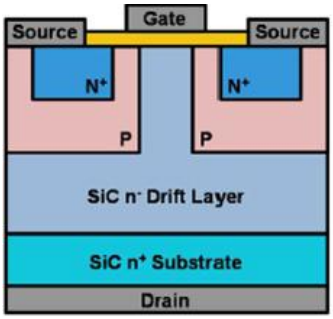


Figure 2.5 SiC-MOSFET structure.

SiC-MOSFETs switch significantly faster than Si-IGBTs, with operating frequencies ranging from *10kHz* to *1MHz*. This results in lower switching losses and higher efficiency in medium-to-high-frequency applications. They exhibit lower on-resistance compared to Si-IGBTs, reducing losses and improving overall system efficiency. Additionally, while they still exhibit reverse recovery effects, their Q_{RR} is significantly lower than that of Si-IGBTs, leading to reduced losses during switching. The combination of lower conduction and switching losses makes SiC-MOSFETs highly efficient. They provide a strong alternative for applications requiring a balance between power handling capability and efficiency. SiC-MOSFETs are more expensive than silicon-based devices due to the issues associated with growing SiC crystals and the high temperatures required for processing. However, ongoing advancements in manufacturing techniques are progressively lowering costs. SiC-MOSFET modules are specifically engineered to minimize parasitic inductances (which are particularly detrimental at high switching frequencies) and to enhance thermal management. By enabling high-voltage and high-current operation, they contribute to achieving high power density. Such modules typically include SiC-MOSFETs and SiC power diodes arranged in various configurations, such as half-bridge, full-bridge, and chopper topologies, along with external passive and protection components, allowing for the implementation of a wide range of power conversion architectures.

2.1.3 GaN-HEMT.

Among WBG materials, gallium nitride has emerged as a particularly promising candidate thanks to its intrinsic properties, including high breakdown strength and high electron saturation velocity, which have attracted substantial research interest [15]. Gallium nitride semiconductor devices are available in two main types: enhancement-mode (E-mode or e-GaN) and depletion-mode (D-mode or d-GaN). Enhancement-mode GaN devices operate similarly to conventional MOSFETs, turning on with a positive gate voltage. They exhibit low on-resistance, but the narrow gate drive voltage margin of E-mode GaN devices renders the gate structure vulnerable to over-voltage stress induced by voltage ringing. In contrast, depletion-mode GaN devices are normally-on, meaning they conduct by default and require a negative gate voltage to turn off, this set a challenge for safe operation in power systems [16]. The structure of a GaN transistor is shown in Fig. 2.6

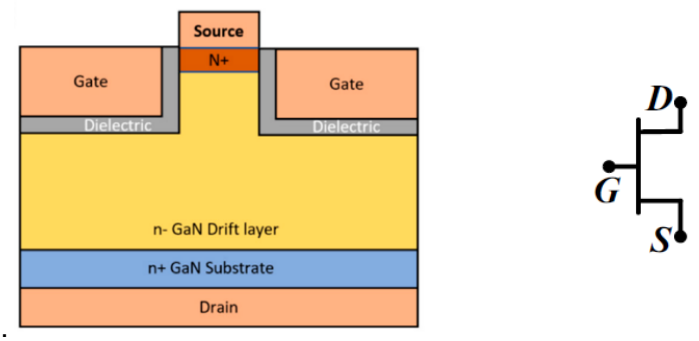


Fig. 2.6 Lateral GaN transistor structure.

One of the major challenges in GaN device fabrication is the lack of commercially available large-diameter native GaN substrates. As a result, GaN layers are typically grown on substrates of silicon, sapphire, or silicon carbide. Among these, SiC is considered the most favorable substrate in terms of device performance and reliability and high-performance GaN-based devices have frequently been demonstrated on SiC substrates [17-19]. However, the growth of high-quality GaN material on SiC substrates remains technically challenging. GaN transistors offer ultra-fast switching, minimal conduction losses, and high efficiency, particularly in high-frequency applications. However, the high drain voltage slew rate can trigger unintended false turn-on events due to the small threshold voltage (typically<*2V*) of these devices [20]. Such parasitic effects may degrade device performance, compromise circuit functionality, and raise significant reliability concerns. GaN technology, while beginning to offer *900V* and *1200V* commercial options, is still technologically immature at these levels, meaning the traditional *650V* rating continues to restrict direct high-voltage applications without multilevel configurations. They operate between *10kHz* and *10MHz*, making them the optimal choice for applications requiring ultra-fast switching. Unlike SiC-MOSFET and Si-IGBT, GaN transistors lack a body diode, eliminating reverse recovery losses altogether and making them particularly well-suited for fast-switching and high-frequency applications. Moreover, currently available GaN transistors feature a lateral structure rather than a vertical one as SiC-MOSFET and Si-IGBT, providing superior high-speed switching and easier integration into circuits, but poorer heat dissipation and use of chip area. The combination of low R_{DSon}, high electron mobility, and elimination of reverse recovery losses results in minimal power dissipation. GaN transistors remain expensive due to their relatively recent introduction to the

market. However, they have an advantage in manufacturing as they can be grown on silicon substrates, allowing integration with existing semiconductor fabrication processes. As large-scale production increases, GaN costs are expected to decrease faster than SiC costs, making GaN more accessible for high-performance applications.

2.2 COMPARISON BETWEEN SI-IGBTS, SIC MOSFETS AND GAN HEMTS.

Future power electronic converters are expected to deliver greater output power while significantly reducing weight and volume [21-22]. An effective strategy to reduce the size of passive elements is to increase the switching frequency. To combine the low conduction losses typical of Si-IGBTs with the low switching losses and high-frequency capabilities of SiC-MOSFETs, WBG semiconductor devices have been introduced. WBG semiconductors-based devices operate at significantly higher voltages, temperatures, and switching frequencies than silicon-based counterparts, leading to increased energy efficiency and reliability in power electronic converters [23-26]. Switching speed is a critical performance metric in power conversion systems. Faster switching not only reduces switching losses but also enables the design of more efficient, lightweight, and compact power converters, factors that are increasingly important in the context of global efforts to address climate change through renewable energy technologies. Currently, the application of Si-based power devices has reached a mature stage. In contrast, WBG devices offer significant advantages in these extreme conditions due to their superior material properties. A comparison of the key characteristics of Si, SiC, and GaN materials is presented in Fig. 2.7 [27].

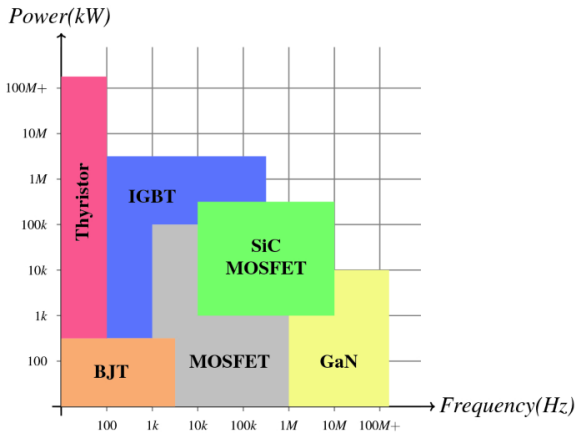


Figure 2.7 Semiconductors technology limitations.

It is evident that WBG materials possess an energy bandgap approximately three times wider than that of Si, enabling power devices based on WBG materials to operate at significantly higher temperatures. Consequently, for the same power level, WBG-based devices exhibit lower conduction losses and reduced temperature sensitivity. Furthermore, the electron saturation drift velocity in WBG materials is approximately twice that of Si, which facilitates higher switching frequencies in power semiconductor devices based on WBG technologies [28-29]. The high-speed switching capabilities of SiC and GaN devices lead to lower heat generation, thereby minimizing the need for bulky thermal management components such as heat sinks. This not only reduces system cost but also contributes to higher power density and more compact designs. Furthermore, the excellent thermal conductivity and high-temperature operation capabilities of SiC and GaN switches allow them to perform reliably without the need for extensive external cooling systems. As a result, power electronic systems based on WBG semiconductors can achieve significant reductions in weight and volume while delivering superior efficiency and reliability. Finally, concerning gate drive circuits, Si-IGBTs demand substantial gate charge and asymmetric bipolar voltages (typically $+15\ V/-15\ V$) that incur high driving losses, their high threshold voltage and slower transients offer a robust noise margin, allowing for forgiving printed circuit board layouts and standard desaturation protection. Conversely, SiC-MOSFETs significantly reduce the gate charge to facilitate higher switching frequencies, yet their rapid transients (with $\frac{dv}{dt}$ exceeding *50* $\frac{V}{ns}$) introduce critical challenges such as

crosstalk and parasitic turn-on via Miller capacitance. Pushing the operational envelope even further, enhancement-mode GaN HEMTs achieve multi-megahertz switching capabilities with negligible gate charge but are constrained by a highly fragile gate structure featuring an ultra-low threshold voltage and strict maximum rating limits (typically requiring a precise $+5\ V$ for turn-on). Ultimately, the adoption of WBG devices enables the realization of highly compact, high-performance power converters with exceptional power density [30-31]. Although wide bandgap devices have demonstrated substantial performance advantages, their widespread adoption in industrial applications remains limited due to high costs and manufacturing process constraints. The historical data indicates that while SiC initially commanded a premium of more than eight times that of Silicon in 2010, the aggressive ramp-up in automotive production is rapidly closing this gap. Projections suggest that by 2030, the difference in component cost will narrow significantly, while system-level costs may actually favor WBG devices due to savings in passive components and cooling requirements. Furthermore, GaN demonstrates the potential to undercut Silicon MOSFET pricing due to its smaller die size for equivalent resistance [32]. Ultimately, the cost of power semiconductor devices reflects a transition from material-limited economics to scale-driven economics; by 2030, the choice between Si, SiC, and GaN will likely be driven almost entirely by technical fit rather than component cost alone [33-34], as shown in fig. 2.8.

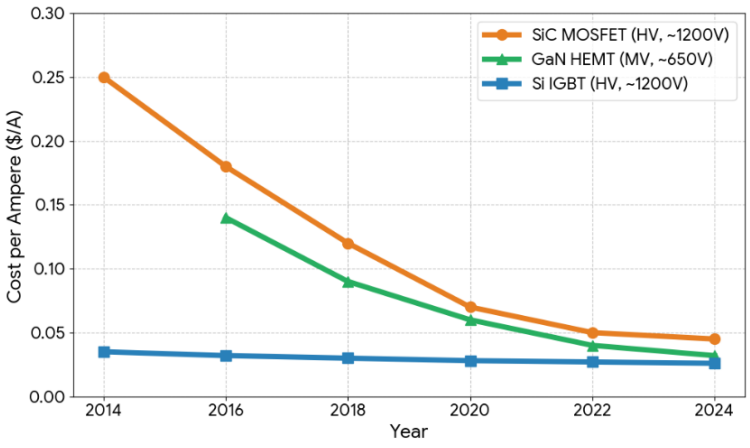
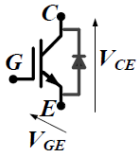
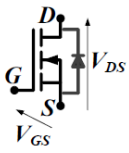
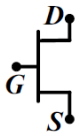


Figure 2.8 Devices cost trends.

Table 2.1 compares the characteristics of Si-IGBTs, SiC-MOSFETs and GaN-HEMTs.

Table 2.1 Semiconductors comparison.

	Si-IGBT	**SiC–MOSFET**	**GaN-HEMT**
			
Conduction Losses	~2.5%	~1.2%	~1%
Switching Losses	~3%	~0.5%	~0.2%
Max Operating Temperature	100°C	600-1000°C	400°C
Switching Frequency	5kHz – 100kHz	10kHz – 10MHz	50kHz – 100MHz
Reverse Recovery Time	100-500ns	10-40ns	0ns
Turn-On/Off Time	50-300ns	10-30ns	4.5-5.7ns
Nominal Voltage	600-6500V	650-3300V	100V-650V
Nominal Current	10-3300A	10-1000A	1-150A
Conduction Loss ($V_{CE(sat)}$/$R_{DS(on)}$)	1.5-3V	10-100mΩ	1-10mΩ
Switching Energy (E_{on}/E_{off})	1mJ-1J	1μJ-1mJ	0.1-1μJ
Efficiency	~95%	~98%	~99%
Cost	Low, with stable trend.	High	High but with rapid decline.

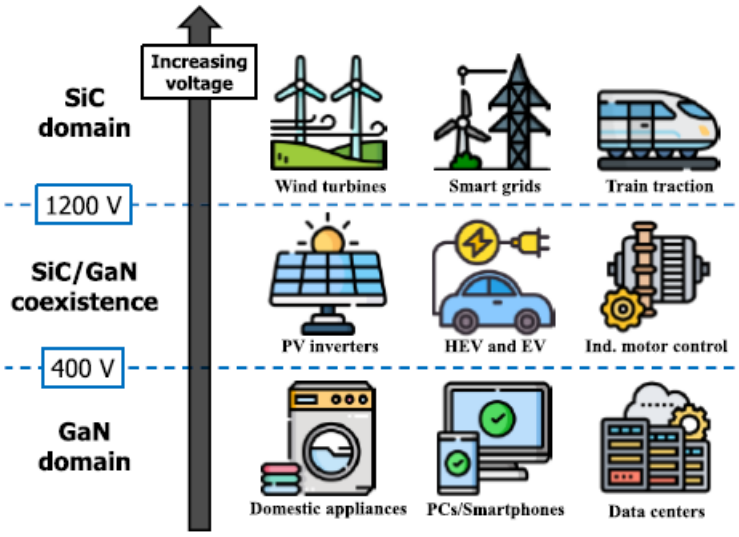


Figure 2.9 Current and future field of interests for SiC and GaN.

The potential application domain of WBG technologies depend largely on the target voltage range, as illustrated in Fig. 2.9.

- <*400V* Applications: Below *400V* GaN is expected to dominate the market. This voltage class includes a wide variety of applications such as domestic appliances, consumer electronics (smartphones, laptops, and their chargers), and power electronics in data centers, where GaN's high-frequency switching and compact size offer significant advantages.
- *400–1200V* Range: In this voltage range, both SiC and GaN are expected to coexist and complement each other, depending on the specific power requirements of the application. This voltage segment encompasses power converters for renewable energy systems, motor drives for industrial automation, and numerous subsystems within the automotive sector. Automotive electrification, in particular, represents a rapidly growing area of interest for WBG technologies. Hybrid and electric vehicles incorporate various power converters and switching devices to manage their electrical subsystems. Here, the ability to reduce converter size and weight while maximizing efficiency is essential for improving driving range, vehicle performance, and overall system integration.

- *>1200V* Applications*:* SiC is expected to play a pivotal role for applications above *1200V*. Key application areas include electric traction for trains, wind turbine converters, and smart grid infrastructure. In the railway sector, where operating voltages can reach up to *5kV* for conventional trains, SiC devices are increasingly viewed as viable alternatives to traditional silicon-based switches, offering enhanced efficiency, reduced losses, and more compact designs. Moreover, SiC holds promise for ultra-high-voltage systems such as those used in high-speed rail, where operating voltages can exceed *25kV*, presenting further opportunities for SiC to displace silicon technologies in demanding power environments.

An in-depth examination of these three technologies is fundamental to fully comprehend the rationale behind their distinct deployment across various application fields, as discussed in the subsequent chapters. Specifically, it was necessary to investigate the physical and material characteristics, the specific application domains of each technology, as well as their market penetration and cost. This foundational knowledge is essential to properly contextualize the subsequent analyses regarding the concurrent use of different device types within the same converter architecture.

2.3 REFERENCE LIST.

[1] W.Shockley, Electrons and Holes in Semiconductors with Applications to Transistor Electronics, D.Van Nostrand, 1950;

[2] C. M. Melliar-Smith, M. G. Borrus, D. E. Haggan, T. Lowrey, A. S. G. Vincentelli and W. W. Troutman, "The transistor: an invention becomes a big business," in *Proceedings of the IEEE*, vol. 86, no. 1, pp. 86-110, Jan. 1998, doi: 10.1109/5.658763;

[3] M. Mohammadi, E. Adib and M. R. Yazdani, "Family of Soft-Switching Single-Switch PWM Converters With Lossless Passive Snubber," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 6, pp. 3473-3481, June 2015, doi: 10.1109/TIE.2014.2371436;

[4] H. Xiao, L. Zhang, Z. Wang and M. Cheng, "A New Soft-Switching Configuration and Its Application in Transformerless Photovoltaic Grid-Connected Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 12, pp. 9518-9527, Dec. 2018, doi: 10.1109/TIE.2018.2826481;

[5] J. Fang, M. Shi, H. Xiao and R. Wang, "A Zero-Voltage-Transition H5-Type Transformerless Photovoltaic Grid-Connected Inverter," in *IEEE Access*, vol. 13, pp. 123110-123119, 2025, doi: 10.1109/ACCESS.2019.2946976;

[6] D. Zheng, Y. Kang, H. Cao, X. Chai, T. Fan and P. Ning, "Monitoring of SiC MOSFET junction temperature with on-state voltage at high currents," in *Chinese Journal of Electrical Engineering*, vol. 6, no. 3, pp. 1-7, Sept. 2020, doi: 10.23919/CJEE.2020.000014;

[7] J. Prakash and M. Veerachary, "Zero-Voltage Zero-Current Transition Network for Dual-Phase Interleaved Converter," in *IEEE Transactions on Industry Applications*, vol. 56, no. 4, pp. 3940-3953, July-Aug. 2020, doi: 10.1109/TIA.2020.2987544;

[8] X. Zhang and G. Sheh, "Implementation of 1.7 kV silicon carbide metal oxide semiconductor field effect transistors in auxiliary power supplies for industrial applications," in *Chinese Journal of Electrical Engineering*, vol. 6, no. 3, pp. 46-55, Sept. 2020, doi: 10.23919/CJEE.2020.000018;

[9] C. N. -M. Ho, H. Breuninger, S. Pettersson, G. Escobar and F. Canales, "A Comparative Performance Study of an Interleaved Boost Converter Using Commercial Si and SiC Diodes for PV Applications," in *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 289-299, Jan. 2013, doi: 10.1109/TPEL.2012.2197830;

[10] X. She, A. Q. Huang, O´ . Luc´ıa and B. Ozpineci, “Review of Silicon Carbide Power Devices and Their Applications,” in IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8193-8205, Oct. 2017, doi: 10.1109/TIE.2017.2652401;

[11] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," in *IEEE Transactions on Electron Devices*, vol. 40, no. 3, pp. 645-655, March 1993, doi: 10.1109/16.199372;

[12] Y. Li *et al*., "State-of-the-Art Medium- and High-Voltage Silicon Carbide Power Modules, Challenges and Mitigation Techniques: A Review," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 14, no. 12, pp. 2177-2195, Dec. 2024, doi: 10.1109/TCPMT.2024.3391653;

[13] A. Marcuzzi, D. Favero, C. D. Santi, G. Meneghesso, E. Zanoni and M. Meneghini, "A Review of SiC Commercial Devices for Automotive: Properties and Challenges," *2023 AEIT International Conference on Electrical and Electronic Technologies for Automotive*

(AEIT AUTOMOTIVE), Modena, Italy, 2023, pp. 1-6, doi: 10.23919/AEITAUTOMOTIVE58986.2023.10217233;

[14] T. Kimoto, "Fundamentals, Commercialization, and Future Challenges of SiC Power Devices," *2023 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK)*, Kyoto, Japan, 2023, pp. 1-4, doi: 10.1109/IMFEDK60983.2023.10366348.

[15] S. Tamura *et al*., "Recent Advances in GaN Power Switching Devices," *2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Monterey, CA, USA, 2010, pp. 1-4, doi: 10.1109/CSICS.2010.5619659.

[16] A. Gutierrez, E. Marcault, C. Alonso and D. Tremouilles, "Experimental Comparison of Discrete Cascode GaN-GaN and Single e-GaN in High-Frequency Power Converter," *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Germany, 2020, pp. 1-5.

[17] L. Gill, S. DasGupta, J. C. Neely, R. J. Kaplar and A. J. Michaels, "A Review of GaN HEMT Dynamic ON-Resistance and Dynamic Stress Effects on Field Distribution," in *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 517-537, Jan. 2024, doi: 10.1109/TPEL.2023.3318182;

[18] M. Wang *et al*., "Advanced Packaging Technology of GaN HEMT Module for High-Power and High-Frequency Applications: A Review," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 14, no. 9, pp. 1537-1550, Sept. 2024, doi: 10.1109/TCPMT.2024.3447079;

[19] M. Tuan Tran *et al*., "A High-Performance GaN Power Module With Parallel Packaging for High-Current and Low- Voltage Traction Inverter Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 13, no. 1, pp. 1188-1209, Feb. 2025, doi: 10.1109/JESTPE.2024.3477743;

[20] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, “An Analytical Model for False Turn-On Evaluation of High-Voltage Enhancement- Mode GaN Transistor in Bridge-Leg Configuration,” IEEE Trans. Power Electron., vol. 32, no. 8 pp. 6416–6433, Aug. 2017;

[21] A. Castellazzi, "Opportunities and challenges of integrated WBG power electronics development," *2021 Third International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, Osaka, Japan, 2021, pp. 1-6, doi: 10.1109/3D-PEIM49630.2021.9497265;

[22] R. Heckman and C. Quinn, "The Growth of Wide Bandgap Technology in Industrial Power Conversion," in *IEEE Power Electronics Magazine*, vol. 11, no. 4, pp. 54-60, Dec. 2024, doi: 10.1109/MPEL.2024.3492294.;

[23] H. A. Mantooth, M. D. Glover and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 374-385, Sept. 2014, doi: 10.1109/JESTPE.2014.2313511;

[24] B. Zhang and S. Wang, "An Overview of Wide Bandgap Power Semiconductor Device Packaging Techniques for EMI Reduction," *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI & PI)*, Long Beach, CA, USA, 2018, pp. 297-301, doi: 10.1109/EMCSI.2018.8495171;

[25] A. Stockman *et al*., "Gate Conduction Mechanisms and Lifetime Modeling of p-Gate AlGaN/GaN High-Electron-Mobility Transistors," in *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5365-5372, Dec. 2018, doi: 10.1109/TED.2018.2877262;

[26] M. Nawaz, N. Chen, F. Chimento and L. Wang, "Static and Dynamic Characterization of High Power Silicon Carbide BJT Modules," in *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 4990-4998, Nov.-Dec. 2016, doi: 10.1109/TIA.2016.2600651;

[27] H. Mhiesan, J. Umuhoza, K. Mordi, C. Farnell and H. A. Mantooth, "Evaluation of 1.2 kV SiC MOSFETs in multilevel cascaded H-bridge three-phase inverter for medium-voltage grid applications," in *Chinese Journal of Electrical Engineering*, vol. 5, no. 2, pp. 1-13, June 2019, doi: 10.23919/CJEE.2019.000007;

[28] Y. Wang, O. Lucia, Z. Zhang, S. Gao, Y. Guan and D. Xu, "A Review of High Frequency Power Converters and Related Technologies," in *IEEE Open Journal of the Industrial Electronics Society*, vol. 1, pp. 247-260, 2020, doi: 10.1109/OJIES.2020.3023691;

[29] M. Gerber, F. Meibody-Tabar and N. Takorabet, "Impacts of Using Wide Bandgap Transistors on Electronics and Motors," *2019 19th International Symposium on Electromagnetic Fields in Mechatronics, Electrical and Electronic Engineering (ISEF)*, Nancy, France, 2019, pp. 1-2, doi: 10.1109/ISEF45929.2019.9096995.;

[30] A. Hu, H. Liu, Y. Zhou, D. Jin, Q. Guo and H. Yang, "Comparative Study on the Characteristics of SiC FET/Si IGBT and SiC MOSFET/Si IGBT Hybrid Switches," 2024 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific), Xi'an, China, 2024, pp. 651-657, doi: 10.1109/ITECAsia-Pacific63159.2024.10738671;

[31] M. Buffolo et al., "Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives," in IEEE Transactions on Electron Devices, vol. 71, no. 3, pp. 1344-1355, March 2024, doi: 10.1109/TED.2023.3346369;

[32] X. Huang, Z. Liu, Q. Li and F. C. Lee, "Evaluation and application of 600V GaN HEMT in cascode structure," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2013, pp. 1279-1286, doi: 10.1109/APEC.2013.6520464;

[33] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155-2163, May 2014, doi: 10.1109/TPEL.2013.2268900;

[34] K. O. Armstrong, S. Das and J. Cresko, "Wide bandgap semiconductor opportunities in power electronics," *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Fayetteville, AR, USA, 2016, pp. 259-264, doi: 10.1109/WiPDA.2016.7799949.

CHAPTER 3

Hybrid (Si/WBG) converters.

3 HYBRID (SI/WBG) CONVERTERS.

3.1 STATE OF THE ART.

As described in [1], power converters play a central role in a wide range of applications, including wind and photovoltaic energy generation [2-4] more-electric aircraft, electric power transmission systems, and hybrid electric vehicles [5-8]. Across all these sectors, the primary design objectives are high efficiency, high power density, and low cost [9-10]. SiC-MOSFETs and Si-IGBTs are widely used as primary switching devices in power electronic converter designs [11-12]. Further increments of power density using Si technology is today impractical, since it is approaching its fundamental physical and material limitations [13-14]. In contrast, WBG semiconductors technologies enable the development of high-performance power converters [15-16]. Although efficiency improvements of only 1–2% can be achieved by using GaN and SiC-based devices, a full replacement of Si devices with WBG alternatives in industrial applications is today unpractical, mostly due to higher costs. Additionally, current commercial WBG devices offer limited voltage and current ratings. Therefore, a hybrid WBG/Si approach could provide a valuable trade-off between performance and cost, achieving substantial efficiency improvements at a moderate cost increment, although introducing certain design issues. Three hybrid WBG/Si approaches can be identified:

- Device-Level Hybridization: Combining WBG and Si devices within a single switching cell to balance conduction and switching performance.
- Module-Level Hybridization: Integrating WBG and Si-based modules within larger converter architectures.
- Circuit-Level Hybridization: Designing converter topologies that assign high-frequency switching tasks to WBG devices and low-frequency operations to Si devices.

Among these approaches, device-level and circuit-level hybridization currently represent the most active areas of research in the field of WBG/Si integration, offering viable pathways toward cost-effective, high-performance power conversion solutions. Indeed, module-level hybridization involves the direct co-packaging Si/WBG connected in parallel within a single physical power module. Operationally, this architecture employs a specialized control strategy where the

fast-switching WBG device is activated specifically during the transient turn-on and turn-off phases to drastically minimize switching losses, whereas the robust Silicon device is utilized to conduct the bulk current during the steady on-state.

According to the device-level hybridization, some switching cells have been developed, where Si and WBG devices operate in parallel to actively support each other. While WBG/Si device-level hybridization shows great promise, it remains primarily in the experimental stage. Overcoming current barriers to practical deployment,such as design methodology, interaction modeling, and control optimization, is essential for industrial adoption.

Dealing with Circuit-Level hybridization various SiC/Si multilevel converter topologies have been proposed, particularly three-level active neutral-point-clamped (3L-ANPC) and five-level (5L-ANPC) converters, aimed at medium-voltage, high-speed drive systems [17-18]. In some configurations, Si-IGBTs are used even for high-frequency switching tasks, but they are operated under soft-switching conditions such as zero-voltage switching (ZVS) or zero-current switching (ZCS) to mitigate switching losses. Experimental comparisons [19-20] show that hybrid topologies employing SiC-MOSFETs for high frequency switching operations generally achieve higher efficiency. This design principle, concentrating all high frequency switching tasks on WBG devices, has proven effective in significantly reducing total switching losses and achieving high overall efficiency.

3.2 WBG FRACTIONAL POWER PROCESSING.

Another such promising approach is the WBG Fractional Power Processing (WFPP) concept, recently introduced to overcome these challenges [21]. The WFPP strategy enables the use of WBG devices to process only a fraction of the total converter power, thereby preserving the high-frequency advantages of a full-WBG design while significantly reducing the overall component cost. This approach offers a viable path for integrating WBG technology into high-current converter applications in a more economical and scalable manner. The concept of the WFPP architecture enables a reduction in component costs by leveraging WBG devices rated for only a fraction of the total converter power, while still retaining the high-frequency (HF) performance benefits typically associated with full WBG-based designs. As illustrated in Fig. 3.1, the WFPP architecture contrasts with conventional all-WBG or all-silicon designs, which rely on a single

power processing path operating at a uniform PWM frequency. In the WFPP approach, power conversion is divided into two parallel paths: a low-frequency (LF) base power processing path utilizing cost-effective silicon devices, and a high-frequency, high-performance fractional power active filter path based on WBG devices. By appropriately coordinating the LF base power path and the HF fractional power path, the overall system can achieve power quality and efficiency levels comparable to those of a full WBG implementation, while significantly reducing the overall cost of components. Based on this principle, [22-23] investigated three-phase Si/SiC hybrid inverters composed of two sub-inverters: a full-power silicon-based inverter and a fractional power WBG-based inverter. Their design achieved high power quality with notably reduced cost. Further contributions [24-25] explored a hybrid-frequency parallel Si/SiC inverter system that incorporated ripple compensation to enable rapid dynamic response. Nevertheless, these WFPP implementations have largely been topology-specific and do not yet offer a generalized methodology applicable to a broader range of converter configurations or application domains. Moreover, prior research on WFPP has primarily focused on experimental validation of selected case studies, with limited exploration of the fundamental cost–performance trade-offs inherent to the WFPP concept.

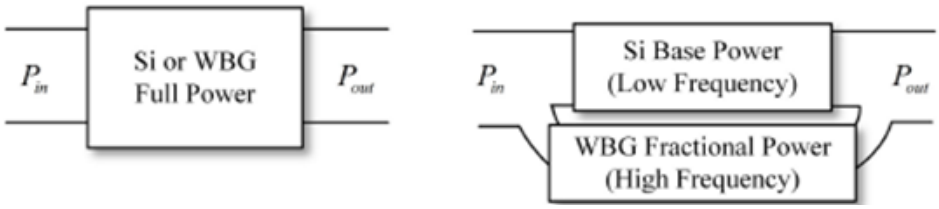


Figure 3.1 (left) Conventional full power processing; (right) WBG fractional power processing.

For example, in [26] authors proposed a generalized WBG/Si Hybrid Half-Bridge (HHB) power processing architecture. As depicted in Fig. 3.2, the half-bridge (HB) circuit is one of the most fundamental building blocks in virtually all power converter topologies. By replacing the conventional HB stage with the proposed HHB, the WFPP concept can be easily integrated into a wide range of converter designs.

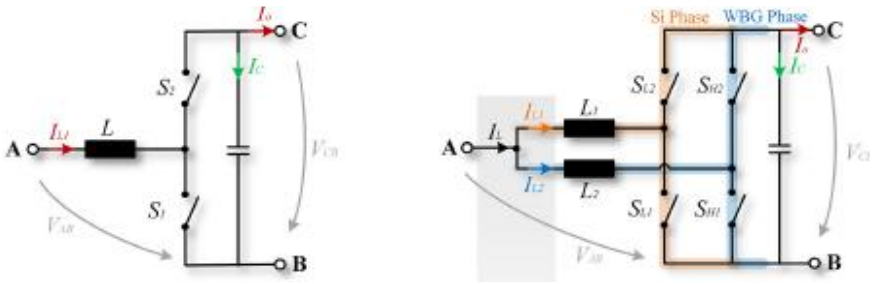


Figure 3.2 (left) Conventional full power half-bridge; (right) Mixed half-bridge.

The proposed HHB comprises two distinct branches: a base power phase utilizing silicon devices to provide high power-handling capability at a low cost, and a fractional power phase employing wide-bandgap devices to enhance efficiency and power quality, with only modest cost overhead. It also features two inherently different phases that utilize distinct semiconductor technologies, switching frequencies, and power ratings. One such hybrid approach [27] involves a Si/GaN configuration, wherein GaN devices are responsible for high frequency switching operations, while Si devices handle the bulk of the current conduction. This division of tasks enables the converter to benefit from the fast-switching characteristics of GaN and the low conduction losses and affordability of Si. This strategy has been investigated across a range of applications. In AC systems, this hybrid concept has been applied to single-phase five-level flying capacitor multilevel inverters [28] and T-type three-level traction inverters for electric vehicles [29]. In the DC domain, hybrid Si/WBG configurations have also been explored in the development of cost-effective and efficient DC-DC converters [30-31]. Within this context, the CHB multilevel inverter emerges as a particularly advantageous topology compared to conventional three-level inverter-based grid integration schemes [32]. The CHB inverter offers modular design, scalability, lower harmonic distortion, and the capability for independent voltage control, making it a strong candidate for applications such as renewable energy systems, electric mobility, and medium-voltage grid interfaces

3.3 HYBRID OPEN-END WINDING CONVERTER.

The core objective underlying this thesis is to propose and validate advanced converter topologies capable of leveraging the concurrent, synergistic operation of WBG/Si devices within the same power conversion system. As demonstrated

in the previous section, a highly promising approach to bypass this dichotomy involves an asymmetric system design. In this paradigm, a primary Si-based inverter processes the bulk active power at a fundamental or low switching frequency, effectively minimizing switching losses in the slower devices. Simultaneously, a secondary, lower-power WBG-based converter operates at a high switching frequency, acting as an active filter to synthesize the desired output current ripple and enhance power quality [33].

By adopting this functional decoupling, WBG devices are strategically utilized strictly where their impact on efficiency and harmonic mitigation is maximized, capitalizing on the inherently low switching losses of this semiconductor category without incurring the prohibitive costs of a full-WBG system [34]. Consequently, within the scope of these hybrid modulation strategies, the OEW topology emerges as a decidedly advantageous solution. By driving a load from both ends using dual inverters, the OEW configuration naturally accommodates the disparate voltage and frequency levels of the Si and WBG stages. It eliminates the need for bulky isolation transformers, increases the effective number of voltage levels, and provides an ideal structural framework for implementing the aforementioned strategies [35].

In-depth discussions regarding the mathematical modeling and control of these architectures will be deferred to the following chapters, wherein the deployment of this hybrid OEW converter topology will be rigorously investigated across diverse, high-impact applications: renewable energy generation, electric vehicles, and Flexible AC Transmission Systems (FACTS). For each domain, the research will focus on both the theoretical development of the modulation strategies and the subsequent hardware implementation of laboratory prototypes. Specifically, the experimental validation will evaluate the system's advantages and disadvantages through a multi-objective lens, focusing on costs, implementation complexity and overall system efficiency across varying load profiles.

Furthermore, while the Si/WBG hybrid approach holds considerable, immediate potential for bridging the performance-cost gap in next-generation power electronics, its commercial adoption in large-scale, high-power applications is expected to remain incremental. The integration of devices with vastly different switching transients and thermal behaviors introduces unique challenges in terms of electromagnetic interference (EMI) and localized thermal management

[36]. Therefore, continued advancements in device manufacturing, cost reduction strategies, and, most crucially, system-level design optimization and advanced digital control will be essential for realizing the full, disruptive promise of Si/WBG hybrid converters in practical industrial applications.

3.4 REFERENCE LIST.

[1] L. Zhang, Z. Zheng and X. Lou, "A review of WBG and Si devices hybrid applications," in *Chinese Journal of Electrical Engineering*, vol. 7, no. 2, pp. 1-20, June 2021, doi: 10.23919/CJEE.2021.000012;

[2] D. Barater, C. Concari, G. Buticchi, E. Gurpinar, D. De and A. Castellazzi, "Performance Evaluation of a Three-Level ANPC Photovoltaic Grid-Connected Inverter With 650-V SiC Devices and Optimized PWM," in *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2475-2485, May-June 2016, doi: 10.1109/TIA.2016.2514344;

[3] H. Tiismus, V. Maask, V. Astapov, T. Korõtko and A. Rosin, "State-of-the-Art Review of Emerging Trends in Renewable Energy Generation Technologies," in *IEEE Access*, vol. 13, pp. 10820-10843, 2025, doi: 10.1109/ACCESS.2025.3528640;

[4] P. Roy, J. He, T. Zhao and Y. V. Singh, "Recent Advances of Wind-Solar Hybrid Renewable Energy Systems for Power Generation: A Review," in *IEEE Open Journal of the Industrial Electronics Society*, vol. 3, pp. 81-104, 2022, doi: 10.1109/OJIES.2022.3144093;

[5] T. Tintu George and A. Sahayadhas, "A Review on Drive Selection, Converters and Control for Electric Vehicle," *2023 IEEE 3rd International Conference on Technology, Engineering, Management for Societal impact using Marketing, Entrepreneurship and Talent (TEMSMET)*, Mysuru, India, 2023, pp. 1-7, doi: 10.1109/TEMSMET56707.2023.10150166;

[6] H. V. Nguyen, D. -C. Lee and F. Blaabjerg, "A Novel SiC-Based Multifunctional Onboard Battery Charger for Plug-In Electric Vehicles," in *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5635-5646, May 2021, doi: 10.1109/TPEL.2020.3026034;

[7] J. Guo *et al*., "A Comprehensive Analysis for High-Power Density, High-Efficiency 60 kW Interleaved Boost Converter Design for Electrified Powertrains," in *IEEE Transactions on Vehicular Technology*, vol. 69, no. 7, pp. 7131-7145, July 2020, doi: 10.1109/TVT.2020.2991395;

[8] W. Chen, Y. Yan, Y. Qi, M. Huang and W. Li, "Recent Development of Aircraft Electric Propulsion System: A Technical Review," in *CES Transactions on Electrical Machines and Systems*, vol. 9, no. 1, pp. 115-130, March 2025, doi: 10.30941/CESTEMS.2025.00004;

[9] M. Antoniou, "Power Semiconductor Devices: From Silicon to Wide Bandgap [Women in Electron Devices]," in *IEEE Electron Devices Magazine*, vol. 2, no. 4, pp. 20-21, Dec. 2024, doi: 10.1109/MED.2024.3513012;

[10] M. Buffolo *et al*., "Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives," in *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1344-1355, March 2024, doi: 10.1109/TED.2023.3346369.

[11] A. Albanna, A. Malburg, M. Anwar, A. Guta and N. Tiwari, "Performance comparison and device analysis Between Si IGBT and SiC MOSFET," *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, USA, 2016, pp. 1-6, doi: 10.1109/ITEC.2016.7520242.

[12] L. Han, L. Liang, Y. Kang and Y. Qiu, "A Review of SiC IGBT: Models, Fabrications, Characteristics, and Applications," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2080-2093, Feb. 2021, doi: 10.1109/TPEL.2020.3005940;

[13] H. Wang, M. Su and K. Sheng, "Theoretical Performance Limit of the IGBT," in *IEEE Transactions on Electron Devices*, vol. 64, no. 10, pp. 4184-4192, Oct. 2017, doi: 10.1109/TED.2017.2737021;

[14] K. Sheng, B. W. Williams, X. He, Z. Qian and S. J. Finney, "Measurement of IGBT switching frequency limits," *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, Charleston, SC, USA, 1999, pp. 376-380 vol.1, doi: 10.1109/PESC.1999.789031;

[15] J. He, T. Zhao, X. Jing and N. A. O. Demerdash, "Application of wide bandgap devices in renewable energy systems - Benefits and challenges," *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, Milwaukee, WI, USA, 2014, pp. 749-754, doi: 10.1109/ICRERA.2014.7016485.;

[16] Abdulhassan, A. K. (2026). Comparative Analysis and Performance Optimization of SiC and GaN Wide Bandgap Semiconductors in Next-Generation Power Converters. *European Journal of Applied Science, Engineering and Technology*, *4*(1), 194-203. https://doi.org/10.59324/ejaset.2026.4(1).12;

[17] L. Zhang *et al*., "A Si/SiC Hybrid Five-Level Active NPC Inverter With Improved Modulation Scheme," in *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4835-4846, May 2020, doi: 10.1109/TPEL.2019.2944688. Q. Guan et al., “An extremely high efficient three-level active neutralpoint- clamped converter comprising SiC and Si hybrid power stages,” IEEE Trans. Power Electron., vol. 33, no. 10, pp. 8341–8352, Oct. 2018;

[18] Q. -X. Guan *et al*., "An Extremely High Efficient Three-Level Active Neutral-Point-Clamped Converter Comprising SiC and Si Hybrid Power Stages," in *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8341-8352, Oct. 2018, doi: 10.1109/TPEL.2017.2784821.;

[19] C. Li *et al*., "Space Vector Modulation for SiC and Si Hybrid ANPC Converter in Medium-Voltage High-Speed Drive System," in *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3390-3401, April 2020, doi: 10.1109/TPEL.2019.2934129;

[20] Z. Feng, X. Zhang, S. Yu and J. Zhuang, "Comparative Study of 2SiC&4Si Hybrid Configuration Schemes in ANPC Inverter," in *IEEE Access*, vol. 8, pp. 33934-33943, 2020, doi: 10.1109/ACCESS.2020.2974554.

[21] A. Kundu, R. Na, A. Amir, Y. Zhou, I. P. Brown and Z. John Shen, "WBG Fractional Power Processing: A New Si-SiC Hybrid Voltage Source Inverter Design," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 6226-6231, doi: 10.1109/ECCE44975.2020.9236129.

[22] M. Basurto, P. Judge, M. Merlin and S. Finney, "Investigation of output filter topologies for a Parallel Hybrid Converter based on Si-IGBTs and partially-rated SiC-MOSFETs," *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, Aalborg, Denmark, 2020, pp. 1-7, doi: 10.1109/COMPEL49091.2020.9265661;

[23] P. D. Judge and S. Finney, "2-Level Si IGBT Converter with Parallel Part-Rated SiC Converter Providing Partial Power Transfer and Active Filtering," *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, Canada, 2019, pp. 1-7, doi: 10.1109/COMPEL.2019.8769710;

[24] J. Endres and A. Ackva, "A parallel three-phase converter system for ripple current compensation and passive filter reduction," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, Switzerland, 2015, pp. 1-9, doi: 10.1109/EPE.2015.7309135;

[25] T. -F. Wu, Y. -H. Huang and Y. -T. Liu, "3Φ4W Grid-Connected Hybrid-Frequency Parallel Inverter System With Ripple Compensation to Achieve Fast Response and Low Current Distortion," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 11, pp. 10890-10901, Nov. 2021, doi: 10.1109/TIE.2020.3032920;

[26] C. Zhang *et al*., "WBG and Si Hybrid Half-Bridge Power Processing Toward Optimal Efficiency, Power Quality, and Cost Tradeoff," in *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6844-6856, June 2022, doi: 10.1109/TPEL.2021.3138464.

[27] G. Liu, K. H. Bai, M. McAmmond, A. Brown, P. M. Johnson and J. Lu, "Critical short-timescale transient processes of a GaN+Si hybrid switching module used in zero-voltage-switching applications," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, USA, 2017, pp. 93-97, doi: 10.1109/WiPDA.2017.8170528;

[28] K. Qu, C. Zhang, W. Chen, B. Hu, X. Yin and J. Wang, "A Hybrid Si/GaN 5-Level Flying Capacitor Single-phase Inverter and its Current Ripple Analysis," *2020 IEEE 1st China International Youth Conference on Electrical Engineering (CIYCEE)*, Wuhan, China, 2020, pp. 1-6, doi: 10.1109/CIYCEE49808.2020.9332618;

[29] J. Lu, R. Hou, P. Di Maso and J. Styles, "A GaN/Si Hybrid T-Type Three-Level Configuration for Electric Vehicle Traction Inverter," *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Atlanta, GA, USA, 2018, pp. 77-81, doi: 10.1109/WiPDA.2018.8569194;

[30] L. Kou and J. Lu, "A GaN and Si Hybrid Solution for 48V-12V Automotive DC-DC Application," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 2858-2864, doi: 10.1109/ECCE44975.2020.9236097;

[31] D. Liu, Y. Wang, Z. Chen and B. Li, "A Buck Converter with Cost-Effective GaN/Si Hybrid Switches and CRM Operation for High-Efficiency and High-Power-Density Applications," *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, Singapore, 2018, pp. 1-6, doi: 10.1109/SPEC.2018.8635892;

[32] J. -S. Lee, K. -B. Lee and Y. Ko, "An improved phase-shifted PWM method for a three-phase cascaded H-bridge multi-level inverter," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 2017, pp. 2100-2105, doi: 10.1109/ECCE.2017.8096417;

[33] S. De Caro et al., "THD and efficiency improvement in multi-level inverters through an open end winding configuration," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 2016, pp. 1-7, doi: 10.1109/ECCE.2016.7855496;

[34] D. Woldegiorgis, M. M. Hossain, Z. Saadatizadeh, Y. Wei and H. A. Mantooth, "Hybrid Si/SiC Switches: A Review of Control Objectives, Gate Driving Approaches and Packaging Solutions," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 2, pp. 1737-1753, April 2023, doi: 10.1109/JESTPE.2022.3219377;

[35] Zerdani, Mohammed, Sid Ahmed El Mehdi Ardjoun, and Houcine Chafouk. 2025. "Overview of Dual Two-Level Inverter Configurations for Open-End Winding Machines: Enhancing Power Quality and Efficiency" *Applied Sciences* 15, no. 10: 5611. https://doi.org/10.3390/app15105611;

[36] P. H. G. Vilela, E. F. Cota, H. A. Pereira, T. P. Corrêa, and A. F. Cupertino, “Towards a next-generation hybrid switch: Challenges and insights on the parallelization of SiC-MOSFET and Si-IGBT”, Eletrônica de Potência, vol. 30, p. e202523, Mar. 2025.

CHAPTER 4

Hybrid OEW converter for wind generators.

This chapter is extensively based on the following publications:

G. Baia et al., "An Open-End Winding Wind Generator with Integrated Energy Storage," 2023 International Conference on Clean Electrical Power (ICCEP), Terrasini, Italy, 2023, pp. 260-266, doi: 10.1109/ICCEP57914.2023.10247441.

G. Baia et al., "Efficiency and Economic Analysis of Open-End Winding Converter for Renewable Energy Systems Using Hybrid Silicon-Wide Bandgap Devices." 411-416. 10.1109/ICCEP65222.2025.11143639.

G. Baia et al., "A high efficiency three-port power converter for wind generators with energy storage", Journal of Energy Storage, Volume 116, 2025, 116029, ISSN 2352-152X, https://doi.org/10.1016/j.est.2025.116029.

4 HYBRID OEW CONVERTER FOR WIND GENERATORS.

4.1 INTRODUCTION.

The previous chapter highlighted the growing adoption of hybrid multilevel power converters and, particularly, their technological evolution compared to traditional two-level converters. This reduces circulating currents and, consequently, power losses. However, these advantages come at the cost of increased system complexity and a larger number of semiconductor devices, which raise overall investment and maintenance costs.

Wind power is increasingly utilized for electricity generation in both large wind farms and small distributed systems [1-2]. However, its intermittent nature leads to power fluctuations caused by variable wind speeds [3-4]. To mitigate these fluctuations, Energy Storage Systems (ESSs), particularly electrochemical Battery Packs (BPs), are often integrated into wind generation plants [5–10].

Integrating a BP into the conventional power-conversion architecture of a WG, typically composed of an AC/DC controlled rectifier and a grid inverter (GI), or into a PV system, usually consisting of a DC/DC stage and a GI, requires the addition of a bidirectional power converter. The resulting three-port power-conversion structure, illustrated in Fig. 4.1, features two unidirectional ports and one bidirectional port. In this context, multilevel inverters can further increase the power density of such systems by supporting a higher number of ports, thereby eliminating the need for an additional dc–dc battery converter.

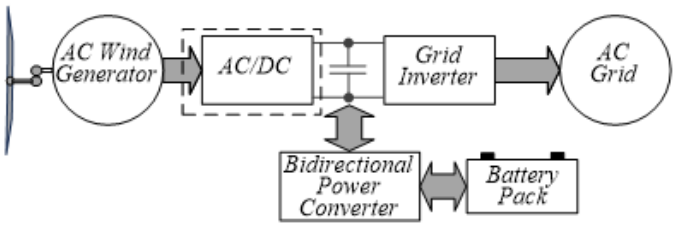


Fig. 4.1 Three-port power converter for a WG integrating a battery pack.

While standard MLIs can enhance power density by accommodating multiple ports, OEW configurations offer a superior alternative to conventional MLI topologies [11-13]. Indeed, as discussed in Chapter 3, OEW structures provide higher power quality with reduced THD, improved fault tolerance, lower voltage stress on the switching devices, and a reduced $\frac{dv}{dt}$ Furthermore, a key structural advantage of the OEW configuration is its ability to seamlessly integrate multiple power ports. This enhances the overall power density of the conversion system and eliminates the need for additional DC-DC converters to manage energy storage, leading to a more streamlined architecture. This chapter examines a specific OEW topology for renewable energy systems, described in detail in [14]. Building on this evidence of superior efficiency over conventional MLIs, the present work investigates how to further enhance the OEW topology's performance by incorporating WBG devices. The back-to-back power converters under analysis include the AC/DC stage for wind generator (WG) applications and the DC/AC stage for the integration with the grid. Moreover, as highlighted in [15], the same topology has already demonstrated excellent overall efficiency in wind-generator operation when GaN devices are used.

4.2 HYBRID POWER CONVERTER FOR WIND GENERATORS WITH INTEGRATED ENERGY STORAGE SYSTEM.

Integrating an ESS within a WG requires the introduction of a dedicated bidirectional power converter, resulting in a three-port structure, as illustrated in Fig. 4.3. Widely adopted configurations for WGs with integrated ESS include the Common DC Bus (C-DC-Bus) and the Common AC Link (C-AC-Link), shown in Fig. 4.4 [16–18].

In these configurations, a Wind Turbine (WT) drives an AC generator connected to a Two-Level PWM Rectifier (TLR-PWM), which feeds a DC bus interfaced to the grid via a Grid Inverter (GI). In the C-DC-Bus configuration, the BP is connected to the DC bus through a bidirectional DC/DC converter, whereas in the C-AC-Link configuration the WT and BP are interfaced with the AC grid through separate inverters [19-21].

To improve efficiency and reduce THD, advanced solutions based on MLCs have been developed. Among these, OEW configurations, such as those depicted in Fig. 4.5, stand out for their high efficiency and enhanced fault tolerance [22-24].

In this context, a novel OEW-based three-port power converter has been developed that integrates a Three-Level T-Type Rectifier (3L-TTR), using Si-IGBTs with a Two-Level Converter (TLC) based on GaN FETs, as illustrated in Fig. 4.4. The 3L-TTR, rated for *800V*, operates at the fundamental frequency to achieve nearly zero switching power losses. Meanwhile, the floating DC bus voltage of the TLC is controlled to allow the use of *650V* GaN devices. Acting as an active power filter, the TLC shapes the AC generator phase current sinusoidally through high-frequency PWM.

This configuration effectively combines GaN and Si-IGBT technologies, delivering the performance of a multilevel PWM inverter fully equipped with *1200V* GaN devices, while employing only *650V* GaN devices in practice. The result is an highly efficient power converter [25–26]. In particular, thanks to the work previously carried out in [27], simulations have confirmed encouraging results regarding the efficiency of the proposed system compared to the presented alternatives. Fig. 4.2 shows the efficiency radar chart of the analyzed systems, obtained by simulations.

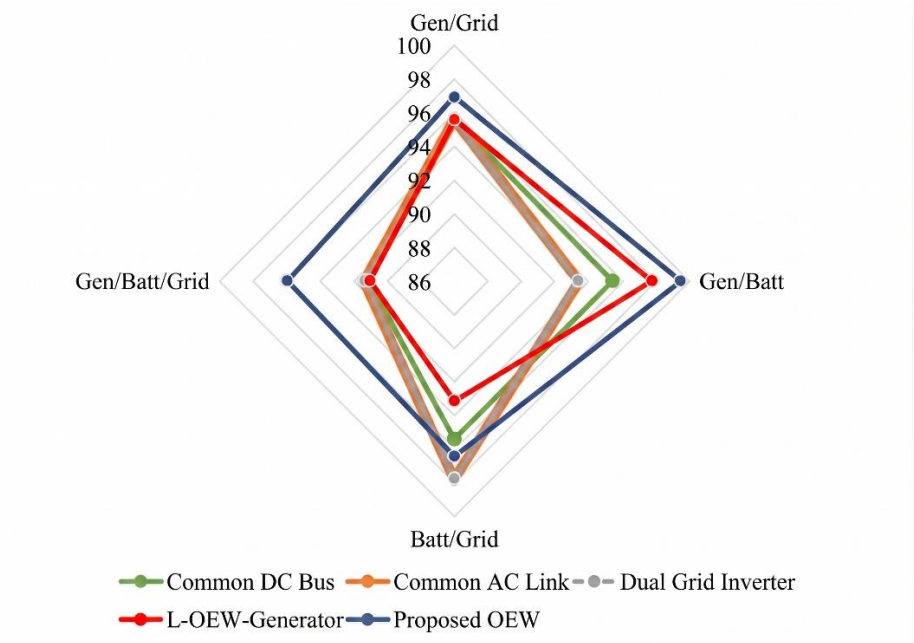
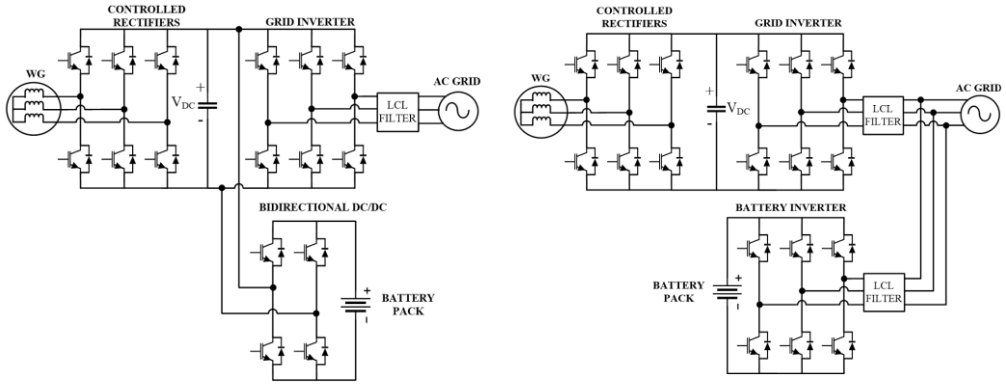
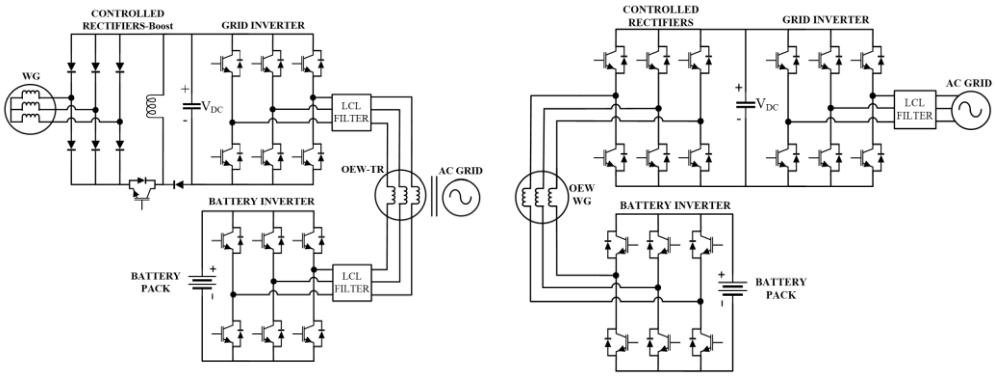


Fig. 4.2 Efficiency radar chart simulation.



(a) (b)

Fig. 4.3 Typical structures of wind generators with batteries. (a) Common DC-Link; (b) Common AC-Link.



(a) (b)

Fig. 4.4 OEW structures for wind generators with batteries: (a) Dual-Grid Inverter, (b) 3 L-OEW-Generator.

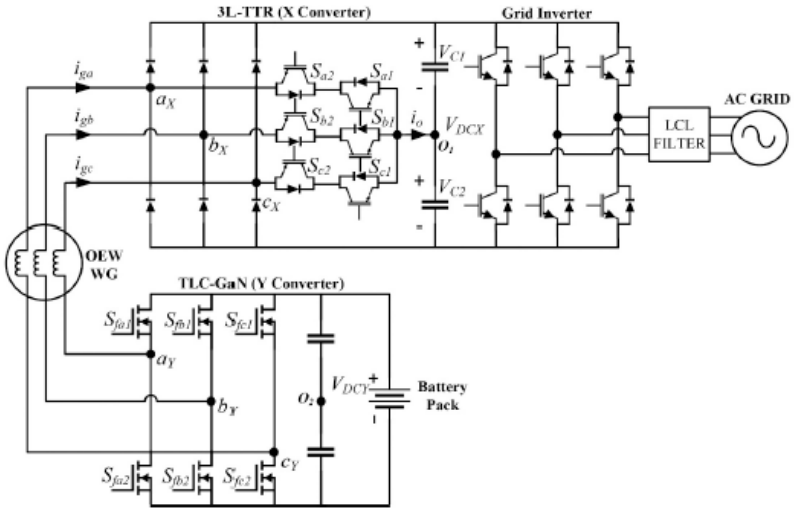


Fig. 4.5 The proposed OEW configuration.

The proposed OEW configuration comprises three main components: a unidirectional three-level T-Type rectifier (3L-TTR, hereafter X converter), a bidirectional two-level converter (TLC, hereafter Y converter), and a two-level GI. As shown in Fig. 4.6, the *j-phase* (*j=a,b,c*) ac-side voltages of converters X and Y, referred to the midpoints O_1 and O_2 of their respective dc buses, are given by

$$V_{jX} = \frac{l_{jX} - 1}{2} V_{DCX}\,, \quad V_{jY} = \frac{2l_{jY} - 1}{2} V_{DCY} \tag{5}$$

where V_{DCX} and V_{DCY} are the dc-link voltages of converters X and Y, respectively. The discrete variables $l_{jX} = 0, 1, 2$ and $l_{jY} = 0, 1$ denote the instantaneous switching states that determine the *j-phase* output voltage levels of converters X and Y.

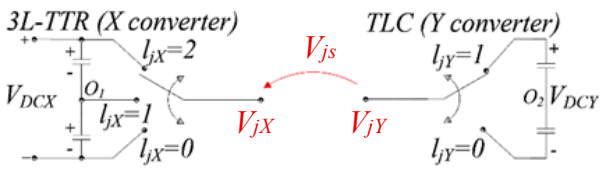


Fig. 4.6 OEW inverter output voltage composition.

Since both converters are supplied by two independent isolated power sources V_{DCX} and V_{DCY}, the machine *j-phase* stator voltage V_{js} is given by:

$$V_{js} = V_{jX} - V_{jY} - V_o \tag{6}$$

being V_o the voltage between the midpoints O_1 and O_2 of the DC buses of the two inverters, which in turn is given by:

$$V_o = \frac{1}{3}(V_{aX} + V_{bX} + V_{cX}) - \frac{1}{3}(V_{aY} + V_{bY} + V_{cY}) \tag{7}$$

According to (5) and (6), the number of potential levels N_{XY} of the voltage $V_{jXY} = V_{jX} - V_{jY}$ is a function of the ratio k_v between the voltages of the two DC buses:

$$k_v = \frac{V_{DCY}}{V_{DCX}} \tag{8}$$

According to (7), also the number of potential levels N_{VO} of the voltage V_o is a function of k_v. As a result, the machine phase voltage V_{js} features N potential levels, as shown in Tab. 4.1.

Table 4.1 Voltage levels v.s. Kv.

k_v	N_{XY}	N_{VO}	N
1	5	9	15
$0.5<k_v<1$	6	13	25
0.5	4	7	11
$0.25<k_v<0.5$	6	13	31
0.25	6	9	19
$k_v<0.25$	6	13	31

According to (6) and (8), and Table 4.1, the voltage ratio k_v plays a crucial role in the proposed system because it directly influences key performance aspects such as the voltage and current THD and the voltage ratings of the devices of the Y-converter. In general, increasing k_v raises the voltage to be sustained by the devices of the Y-converter and their switching losses, whereas choosing k_v too low can deteriorate the generator phase-current waveform and/or cause oscillations of the dc-bus voltage.

4.2.1 X converter operation and control.

The X converter adopts a high-efficiency 3L-TTR topology in which all power devices operate at the fundamental frequency to minimize switching power losses. Unlike a conventional Vienna rectifier, where current shaping is achieved by high-frequency switching of the three bidirectional switches, in the proposed configuration this task is instead assigned to the bidirectional Y converter. The absence of high-frequency operations makes the use of fast-switching devices unnecessary, allowing the use of low on-state-loss Si-IGBTs. Considering the structure shown in Fig. 4.6, which depicts only the X converter connected to the GI, the X converter is controlled using a Step Modulation (SM) strategy defined by the switching rules listed in Table 4.2.

Assuming a constant DC-bus voltage V_{DCX}, regulated by the GI, the AC-side voltage waveform V_{jX} exhibits three discrete levels, as illustrated in Fig. 4.6. The Fourier series expansion of V_{jX} is expressed as:

$$\begin{aligned} V_{jX} &= V_{1jX} + V_{hjX} \\ V_{1jX} &= \frac{2V_{DCX}}{\pi}\cos(\alpha)\sin(\theta_e) \\ V_{hjX} &= \sum_{h=5,7,11..}^{Nmax}\left(\frac{4V_{DCX}}{h\pi}\cos(h\alpha)\sin(h\theta_e)\right) \end{aligned} \quad (\mathbf{9})$$

where N_{max} is the order of the highest voltage harmonic that the Y converter is required to compensate, V_{1jx} is the fundamental component of V_{jX}, α the switching angle, θ_e is the generator voltage phase angle, h the harmonic order, while V_{hjX} represents the *h-th* harmonic component. According to Fig 4.7, the conduction of diodes D_{j1} and D_{j2} depends on the instantaneous value of the fundamental component V_{1jx} of the AC generator voltage. Specifically, for diode D_{a1} it is possible to write:

$$V_{Da1} = V_{DCX} - V_{1aX} + V_{1bX} = V_{DCX} - V_{1abX} \quad (\mathbf{10})$$

The necessary condition for the diode D_{a1} to conduct is that $V_{Da1}<0$, thus:

$$V_{1abX} > V_{DCX} \quad (\mathbf{11})$$

where V_{1abX} is the line-to-line output voltage of the X converter. For a Low Voltage Grid (LVG) rated at *400V* and *50Hz*, the DC link voltage V_{DCX}

should be set to at least *700V*. This means that the peak value of the generator's phase voltage must exceed *404V* to ensure diode conduction.

In wind-turbine (WT) applications, two types of generators are commonly used:

- Low-voltage machines (<*50kW*), rated at *400V*: the peak value of the stator voltage is about *325V*, which is lower than *404V*, potentially leading to malfunction.
- Medium-voltage machines (>*50kW* up to *10MW*), rated at *690V*: the peak phase stator voltage reaches approximately *563V*, which is higher than *404V* and therefore suitable.

The fundamental voltage V_{1jx} can be regulated by adjusting the switching angle α, which also determines the zero-voltage level, as described in (9). It should be noted that the minimum value of *α* is constrained by the difference between the given peak value of the stator voltage V_{1jx} and $V_{DCX}/2$. From this minimum, the switching angle can only be increased to reduce the fundamental voltage V_{1jx}, which in turn limits the controllable power range. To overcome these limitations, the Y converter is employed to boost the AC-side voltage of the X converter, particularly beneficial for low-power WTs (<*50kW*), and to control the generator current.

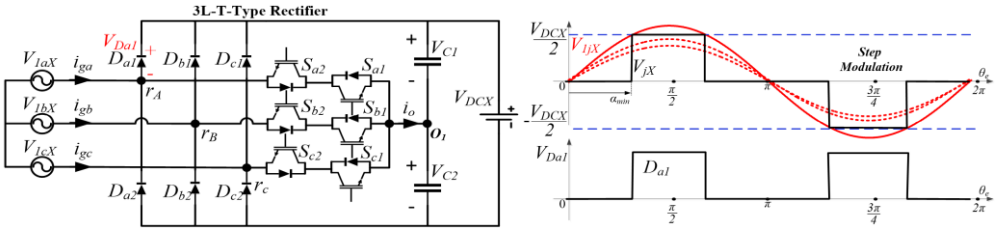


Fig. 4.7 (left) X Converter connection to GI; (right) X Converter AC side voltage waveform and voltage limits.

Considering a Permanent Magnet Synchronous Generator (PMSG), the amplitude of stator voltage $|V_{1js}|$ is obtained from the mathematical model of the generator in the rotating dq-axes reference system as:

$$|V_{1js}| = \sqrt[2]{V_{qs}^2 + V_{ds}^2} \qquad (12)$$

being:

$$V_{qs} = R_s i_{qs}^* + L_q \omega_{re} i_{ds}^* + \omega_{re} \lambda_{PM}$$
$$V_{ds} = R_s i_{ds}^* - L_d \omega_{re} i_{qs}^* \quad (13)$$

where i_{qds}^* are the qd-axes components of reference stator currents, L_{qd} the qd-axes inductances, λ_{PM} the flux of the permanent magnet and ω_{re} the rotor speed. The voltage phase angle q_e is obtained as:

$$\theta_e = \theta_r + tan^{-1}\left(\frac{V_{qs}}{V_{ds}}\right) \quad (14)$$

being θ_r the rotor shaft angular position. As will be explained in follow, the switching angle α is selected to regulate the battery power.

Table 4.2 X converter switching rules.

X CONVERTER - POLE a		
$\alpha_{min}<\theta_e<\alpha$ $\pi-\alpha < \theta_e < \pi+\alpha$ $2\pi-\alpha < \theta_e <2\pi$	$i_{ga}>0$	**I_{aX}=1** (S_{a1} ON - S_{a2} OFF)
	$i_{ga}<0$	**I_{aX}=2** (S_{a1} OFF - S_{a2} ON)
$\alpha < \theta_e < \pi-\alpha$ $\pi+\alpha < \theta_e <2\pi-\alpha$		**I_{aX}=0** (S_{a1} OFF - S_{a2} OFF)
X CONVERTER - POLE b		
$2/3\pi < \theta_e <\alpha+2/3\pi$ $5/3\pi-\alpha < \theta_e <5/3\pi+\alpha$ $2/3\pi-\alpha < \theta_e <2/3\pi$	$i_{gb}>0$	**I_{bX}=1** (S_{b1} ON – S_{b2} OFF)
	$i_{gb}<0$	**I_{bX}=2** (S_{b1} OFF – S_{b2} ON)
$\alpha < \theta_e < \pi-\alpha$ $\alpha < \theta_e < \pi-\alpha$		**I_{bX}=0** (S_{b1} OFF - S_{b2} OFF)
X CONVERTER - POLE *c*		
$4/3\pi < \theta_e <\alpha+4/3\pi$ $1/3\pi-\alpha < \theta_e <1/3\pi+\alpha$ $4/3\pi-\alpha < \theta_e <4/3\pi$	$i_{gc}>0$	**I_{cX}=1** (S_{c1} ON - S_{c2} OFF)
	$i_{gc}<0$	**I_{cX}=2** (S_{c1} OFF - S_{c2} ON)
$\alpha < \theta_e < \pi-\alpha$ $\alpha < \theta_e < \pi-\alpha$		**I_{cX}=0** (S_{c1} OFF - S_{c2} OFF)

4.2.2 Y converter operation and control.

The Y converter is driven by a high switching frequency PWM to boost the AC side voltage of the X converter, shape the generator current sinusoidally, and manage the battery pack. Figure 4.8 shows the equivalent circuit of the proposed system. Figure 4.9 shows the phasors of the AC side X converter voltage ($\overrightarrow{V_{1x}}$, $\overrightarrow{V_{1y}}$, $\overrightarrow{V_{1s}}$, $\overrightarrow{i_g}$), AC side Y converter voltage, generator voltage, and stator current, respectively, while X_L represents the reactance of the PMSG.

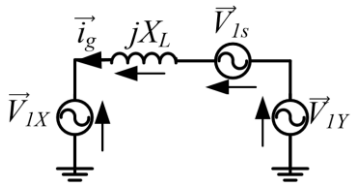


Fig. 4.8 Equivalent circuit of the proposed OEW configuration.

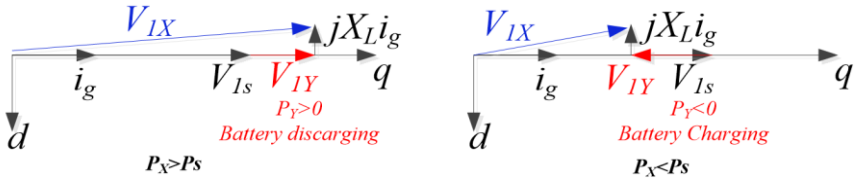


Fig. 4.9 (left) Vector diagrams P_{Grid}>P_{Gen}; (right) Vector diagrams P_{Grid}<P_{Gen}.

The active and reactive powers of X converter, Y converter and AC generator can be written as:

$$P_X = \frac{3}{2}\left(V_{q1X}i_{qs} + V_{d1X}i_{ds}\right) = P_{Grid}$$
$$Q_X = \frac{3}{2}\left(V_{q1X}i_{ds} - V_{d1X}i_{qs}\right) = Q_{Grid} \quad (15)$$

$$P_Y = \frac{3}{2}\left(V_{qY}i_{qs} + V_{dY}i_{ds}\right) = P_{Batt}$$
$$Q_Y = \frac{3}{2}\left(V_{qY}i_{ds} - V_{dY}i_{qs}\right) = Q_{Batt} \quad (16)$$

$$P_{Gen} = \frac{3}{2}\left(V_{qs}i_{qs} + V_{ds}i_{ds}\right)$$
$$Q_{Gen} = \frac{3}{2}\left(V_{qs}i_{ds} - V_{ds}i_{qs}\right) \quad (17)$$

Three possible operations can be identified. In the first operation, the required grid power P_{Grid} equals the generator power P_{Gen}. In this condition, the Y converter acts as an active power filter (APF) and P_{Batt}=0. The second operation occurs when the required grid power exceeds the generator power, while the third operation occurs when the required grid power is lower than the generator power. In the former case, the battery compensates for the insufficient power generated by the wind turbine by discharging. In the latter case, the surplus power generated by the wind turbine is used to charge the battery. All operational points are illustrated in Table 4.3. Figure 4.9 show the phase diagrams for operations 2 and 3. Under Field Oriented Control (FOC), the q-axis component of the stator current regulates the active power, while the d-axis current controls the magnetic flux. For simplicity, when a Surface Permanent Magnet Synchronous Generator (SPMSG) is used, i_d is set to 0. For a given active power P_{Gen} of the generator, obtained by setting i_q, the battery current can be regulated in both scenarios 2 and 3. When transitioning from operation 2 to 3 and vice versa, changing the sign of the battery power P_Y requires adjusting the switching angle α. In fact, when $P_{Grid}<P_{Ge}$, the voltage V_{1X} must be reduced by increasing α, according to (9). Hence, the generator current is regulated by acting on the Y converter, while the battery current is controlled by adjusting the switching angle α. The control algorithm of the proposed OEW system is shown in Figure 4.10. The voltage at the mid-point O_1 of the DC bus of the X converter can be regulated by acting on the current i_0. A positive current i_0 discharges the low-side capacitor, whereas a negative current discharges the high-side capacitor. Capacitor voltage equalization is achieved by periodically connecting each capacitor directly to the wind generator and the Y converter through the midpoint O_1 and the positive or negative terminal of the DC bus. Active voltage equalization can therefore be accomplished by forcing a suitable current i_{qn} to circulate into or out of the midpoint of the DC bus, as described in fig.4.11. In practice, an additional term i_{qn}^*, proportional to the voltage unbalance, is added to the q-axis current reference i_{qg}^* according to the rules listed in Table 4.4, which prevent charging the wrong capacitor or charging both C_1 and C_2 at the same time.

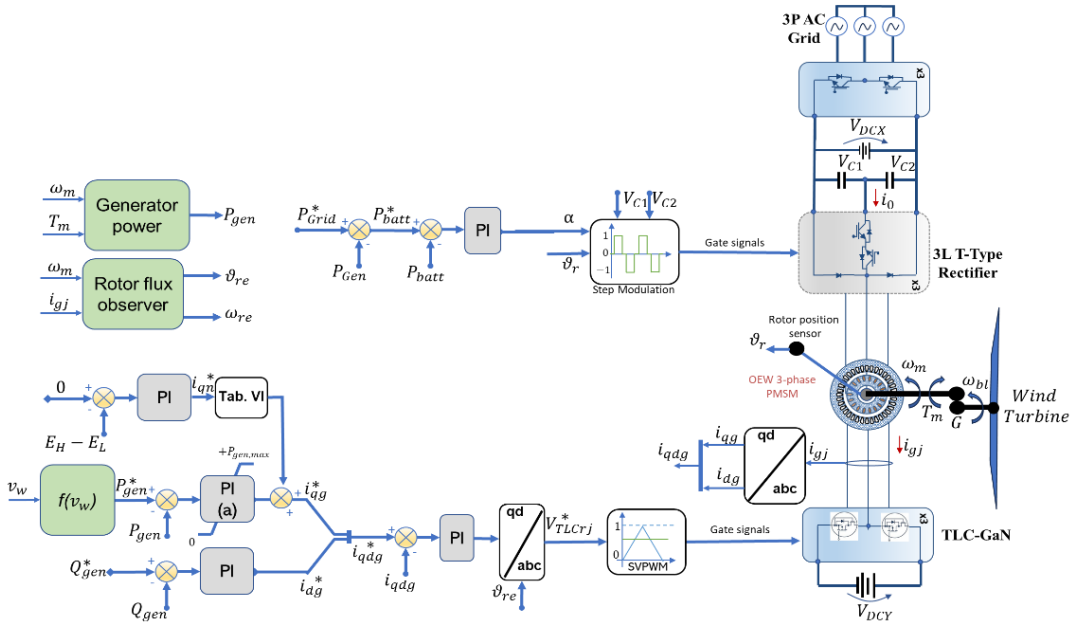


Fig. 4.10 Control algorithm of the proposed OEW system.

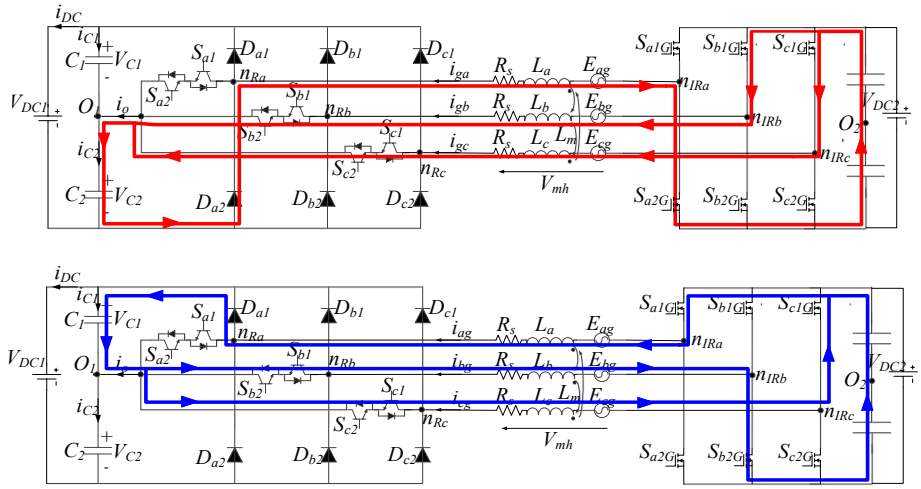


Fig. 4.11 Voltage equalization: $V_{c1} > V_{c2}$ (up), $V_{c1} < V_{c2}$ (down).

Table 4.3 OEW inverter operations.

Operation	P_{batt}*	SOC	APF	Balancing
$P_{Grid} = P_{Gen}$	P_{Batt}*= 0	Unchanged	yes	yes
$P_{Grid} > P_{Gen}$	P_{Batt}*> 0	Discharge	yes	yes
$P_{Grid} < P_{Gen}$	P_{Batt}*< 0	Charge	yes	yes
P_{Batt}*= P_{Grid} - P_{Gen}				

Table 4.4 Dc bus voltages equalization rules.

i_{qn}^* is added to i_{qg}^* **if**	$V_{C1}>V_{C2}$ **and**	$i_{ag}<0$ **and** (S_{b1} ON or S_{c1} ON) **or** $i_{bg}<0$ **and** (S_{a1} ON or S_{c1} ON) **or** $i_{cg}<0$ **and** (S_{a1} ON or S_{b1} ON)
	$V_{C1}<V_{C2}$ **and**	$i_{ag}>0$ **and** (S_{b2} ON or S_{c2} ON) **or** $i_{bg}>0$ **and** (S_{a2} ON or S_{c2} ON) **or** $i_{cg}>0$ **and** (S_{a2} ON or S_{b2} ON)

4.2.3 Selection of the battery voltage.

According to (6) and (9) the AC generator phase voltage is given by:

$$V_{js} = V_{1jX} + V_{hjX} - V_{jY} - V_o \qquad (\mathbf{18})$$

The AC generator phase voltage V_{js} must be made equal to V_{1jX} for achieving a sinusoidal phase current. Hence, in principle, V_0 and the harmonics generated by the X converter low frequency modulation, must be compensated by suitably acting on V_{jY}. However, according to (7) the V_0 waveform features two groups of harmonics, those at frequencies multiple of three times the switching frequency of the X converter and those at frequencies multiple of three times the switching frequency of the Y converter. Since the X converter is operated at the generator fundamental frequency, the first group of harmonics does not lead to correspondent harmonics of the phase current, thus can be neglected. The second group of harmonics can be neglected too, as they give a negligible

contribution to the phase current due to their high frequency. Hence, to shape sinusoidally the phase current only the voltage harmonics caused by the X converter low frequency modulation must be eliminated. The current controller that drives the Y converter accomplishes this task. To eliminate low-order harmonics while also controlling at the same time the generator current, the Y converter requires an appropriate DC bus voltage V_{DCY}, determining the BP rated voltage. The minimum Y converter DC bus voltage required to accomplish the harmonic compensation equals the peak value of the term V_{hjX} in (9). Therefore, this term has been computed for different values of N_{max}, as illustrated in Fig. 4.12, where the red trace represents for comparison what achieved for $N_{max}=+\infty$. Figure 4.12 also highlights that an optimal trade-off is achieved between the Y converter DC bus voltage and the phase voltage THDv by setting $N_{max}=13$, leading to a scaling factor $k_v=0.4$. However, the Y converter not only manages harmonic elimination but also controls the generator current and boosts the AC voltage. The rated peak voltage of the considered *20kW* WT is *325V*. Hence, based on (10) and (11), the AC input voltage of the X converter needs to be boosted by at least 100V using the Y converter. Consequently, the DC link voltage of the Y converter must be raised to *400V*, achieving $k_{vopt}=0.57$.

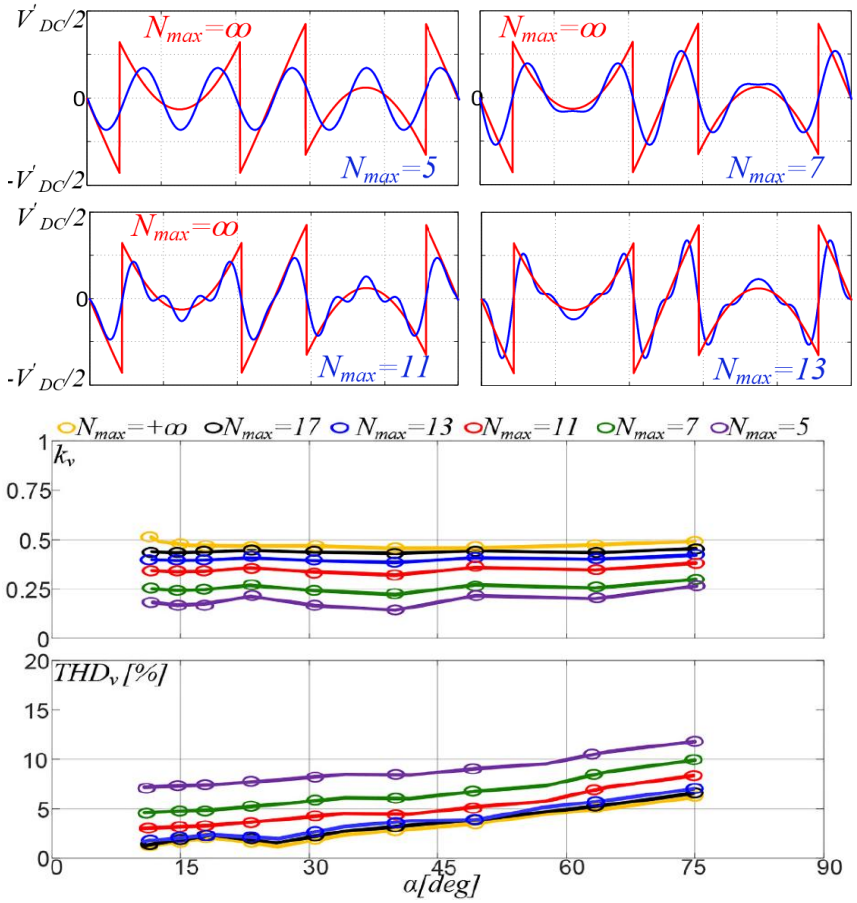


Fig. 4.12 (up)* Waveforms of VhjX v.s. Nmax for α=15°; *(down) Voltage ratio $k_v=V_{DCY}/V_{DCX}$ and THD_v vs. m_{3LI} and N_{max}.

The scaling factor, k_{vopt}, is a crucial parameter in selecting the appropriate battery pack. An *80Ah*, *400V* Lithium-Ion battery is selected, as depicted in Fig. 4.13. This battery is capable of delivering the rated current for two hours while ensuring a voltage ratio above k_{vopt}.

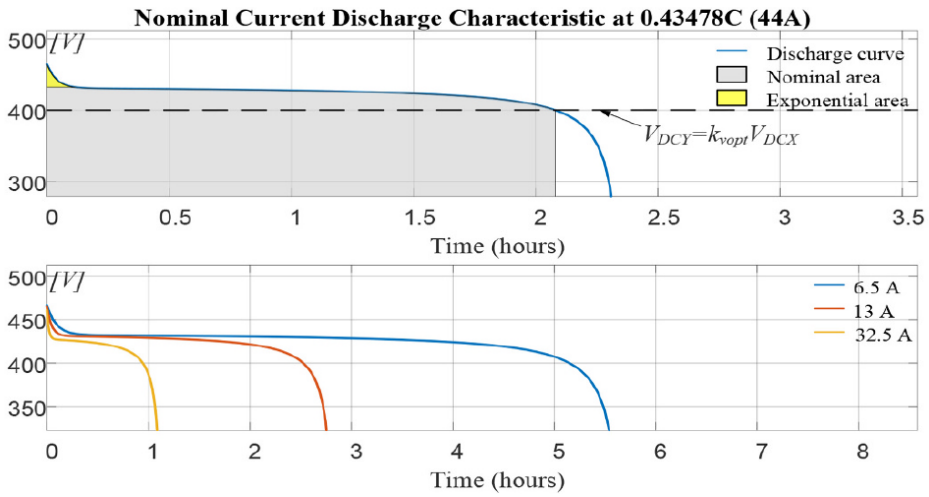
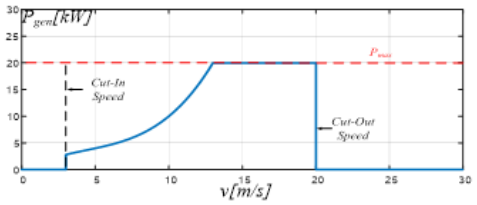


Fig. 4.13 Discharge Characteristics of 80Ah, 400V Lithium-Ion Battery pack.

4.2.4 Simulation of the proposed 20kW OEW system.

A *20 kW* OEW system connected to a LV AC grid rated at *400V* has been simulated. The structure consists of a *20 kW* 3L T-Type converter (X converter), rated at *700V*, a *20kW* TLC converter (Y converter), a *20kW* Permanent Magnet Synchronous Generator (PMSG) and a *20kW* Horizontal Axis Wind Turbine. The X converter is equipped with *1200V*, *50A* Si-IGBTs and operates at the fundamental frequency, whereas the Y converter employs *650V*, *47A* GaN devices. The main parameters of the proposed OEW system are summarized in Tab. 4.5. A Lithium Iron Phosphate (LFP) battery pack was selected due to its capability to provide consistent energy under the variable load conditions typical of wind turbine applications, as well as its significantly lower cost compared to Lithium Titanate (LTO) batteries, which however offer superior cycle life. The sizing of the ESS in a wind-based hybrid power system depends on multiple factors, including load profiles, desired functionalities (grid support or peak shaving), and energy and ancillary service pricing. In this study, a *36kWh* battery pack was chosen to ensure full grid support under the most demanding operating conditions. A DC-link voltage of *400V*, a T-type converter switching frequency of *30kHz*, and a modulation index limit of $N_{max} = 13$ were adopted to achieve an effective phase current shaping across the *0–30kVA* power range. Moreover, the selected switching frequency allows for a fair comparison between the proposed system and conventional power converters based on Si-IGBTs.

Table 4.5 Parameters of the simulated wind power generator.

3 ports OEW power conversion system		**PMSG**	
Rated output power	20kW	Rated power	20kW
Grid port voltage (line to line rms)	400V (3f)	Rated line to line rms voltage	400V (3f V_{ll} RMS)
Generator port voltage (line to line rms)	400V (3f)	Magnetic flux	0.8Wb
Generator port voltage levels	6 (Phase voltage)	Pole pairs	3
Battery port voltage	400V (DC)	Stator inductance	15mH
X Converter (3L T-Type rectifier)		Stator resistance	0.2Ω
Rated power	20kW	Rated speed	102rad/s
Input AC voltage (line to line rms)	400 V	**Wind Turbine**	
Output DC voltage	700V	Type	Horizontal Axis
Number of AC input voltage levels	3 (line to neutral)	Number of blades	3
DC Link Capacitors	2 x 860μF	Rotor diameter	15.8 m
Switching frequency	0-60 Hz	Gear ratio	6
Y Converter (2L inverter)		Rated power	20kW
Rated power	10kW	Rated speed	17rad/s
Input DC voltage	400 V	Cut-in wind speed	3m/s
Output AC voltage (line to line rms)	245 V (3ϕ)	Cut-out wind speed	20m/s
Number of voltage levels	2 (line to neutral)		
DC Link Capacitors	860μF		
Switching frequency	30kHz SVM		
Voltage harmonics eliminated	5^{th}, up to 51^{st}		
Grid inverter			
Rated power	20kW		
Input DC voltage	700 V		
Output AC voltage (line to line rms)	400 V (3ϕ)		
Number of voltage levels	2 (line to neutral)	**Battery Pack Li-Ion (LFP)**	
DC Link Capacitors	860μF	Capacity	80Ah
Switching frequency	30kHz SVM	Rated Voltage	400V

PSIM simulations were carried out to verify the consistency of the control strategy developed for the proposed configuration. Three operating scenarios were analyzed according to the power distribution diagram reported in Tab. 4.3:

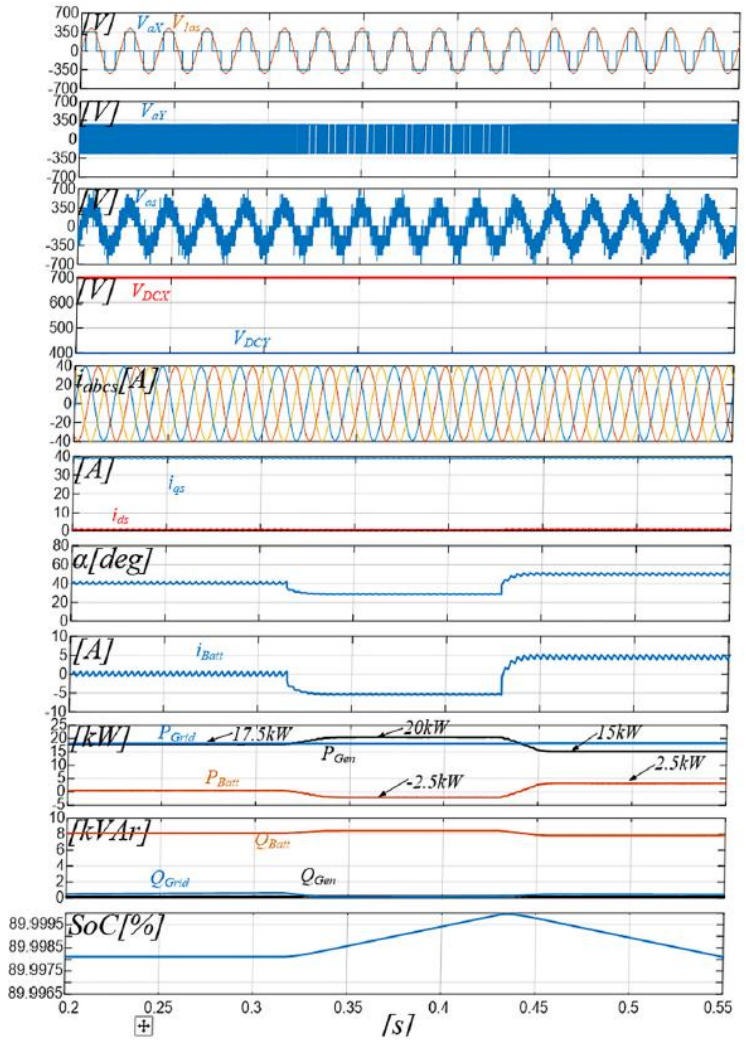
- operation in the constant-power region with a wind speed of *15m/s*;
- operation in the Maximum Power Point Tracking (MPPT) region with a wind speed of *10m/s*;
- operation with the wind turbine inactive.

The simulation presented in Fig. 4.14a focuses on power flow management between the generator, the battery, and the grid, with the generator operating at *102rad/s* under a *15m/s* wind speed. The results illustrate the X converter AC voltage V_{aX}, its fundamental component V_{1aX}, the Y converter AC voltage V_{aY}, the stator voltage V_{as}, the DC-link voltages $V_{DCX}$and V_{DCY}, the stator currents in both $abc$and dqreference frames ($i_{abc,s}$, $i_{qd,s}$), the switching angle α, the battery current i_{Batt}, the grid and generator active/reactive powers ($P_{grid}, Q_{grid}, P_{gen}, Q_{gen}$), and the battery state of charge (SoC).

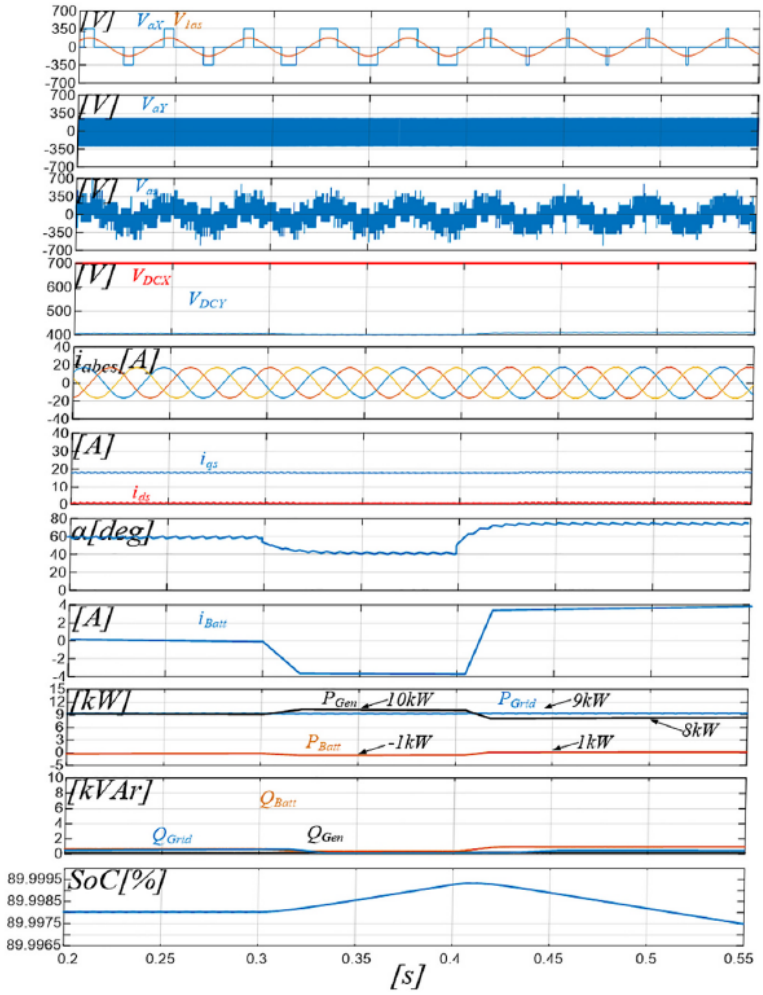
Initially, the *17.5kW* generator output matches the grid power demand, resulting in no battery power exchange and a constant SoC. At *0.3s*, the wind speed increases to *15m/s*, causing the generator output power to rise from *17.5kW* to *20kW*. Since the grid demand remains constant at *17.5kW*, the excess *2.5kW* is directed to the battery, charging it, as indicated by the rising SoC. At *0.43s*, the wind speed decreases, reducing the generator output to *15kW*, which becomes insufficient to meet the grid demand; consequently, the battery provides the remaining *2.5kW*, leading to a discharge phase.

Figure 4.14b presents the same variables for operation under MPPT control at a *15m/s* wind speed, with the generator rotor speed equal to *60rad/s*. According to eq. 29, at lower rotor speeds the back-EMF decreases, leading to an increase in the switching angle α (from approximately *30°–40°* up to *60°–80°*), while the generator current remains properly shaped. Initially, at *8m/s* wind speed, the *9kW* generator output matches the grid demand, and thus no power is exchanged with the battery, keeping the *SoC* constant. At *0.3s*, an increase in wind speed to *10m/s* raises the generator power to *10kW*; with the grid demand fixed at *9kW*, the surplus *1kW* charges the battery, as shown by the *SoC* increase. By *0.43s*, the wind turbine slows down, decreasing the generator power to *1kW*; as this is below the grid demand, the battery compensates the deficit, resulting in *SoC* depletion.

In the final scenario, depicted in Fig. 4.14c, the wind turbine is assumed to be inactive, either due to insufficient wind speed or for safety reasons (e.g., exceeding the rated wind speed). At *0.375s*, the battery supplies *20kW* to the grid and, thanks to its *36kWh* capacity, is capable of sustaining the load for nearly two hours.



(a)


[V]
V_{aX} V_{las}
[V]
V_{aY}
[V]
V_{as}
[V]
V_{DCX}
V_{DCY}
i_{abes}[A]
[A]
i_{qs}
i_{ds}
α[deg]
[A]
i_{Batt}
[kW]
P_{Gen} 10kW
P_{Grid} 9kW
8kW
P_{Batt} -1kW
1kW
[kVAr]
Q_{Batt}
Q_{Grid}
Q_{Gen}
SoC[%]
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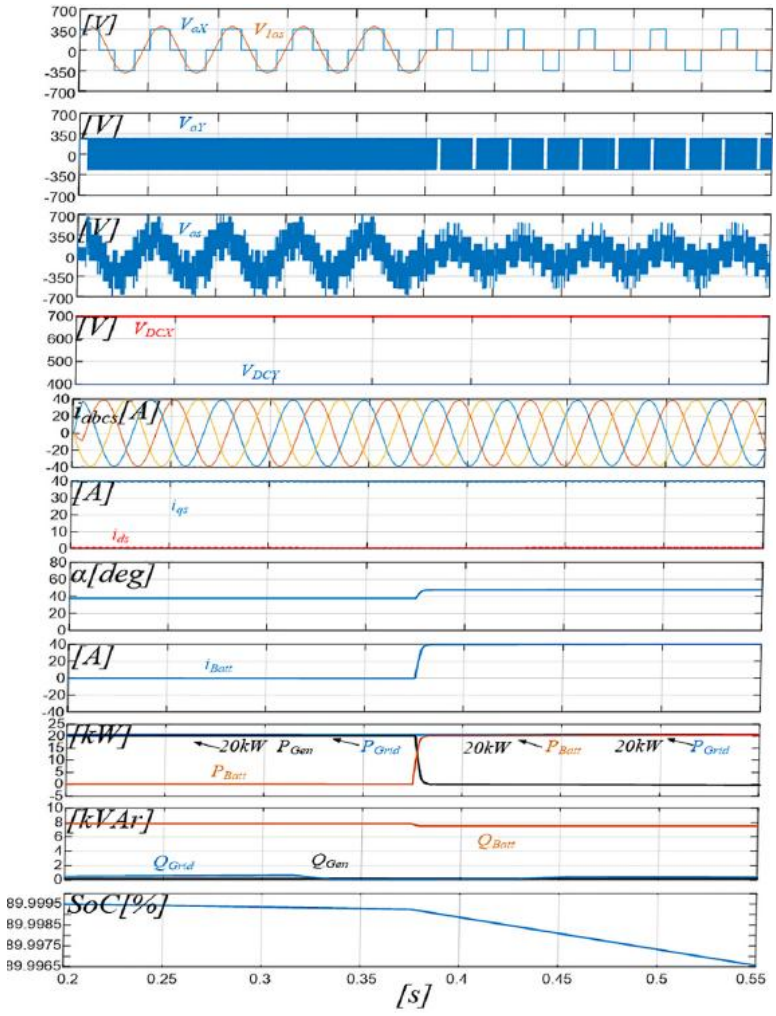
(b)



(c)

Fig. 4.14 (a) Constant power region operation, wind speed 15m/s (20kW); ***(b) MPPT region operation, wind speed 10m/s (10kW); (c) Wind Turbine inactive.***

The performance in equalizing the voltages across *C1* and *C2* is assessed in the simulation of Fig. 4.15, where the generator is spinning at *102rad/s* at 80% of rated current with V_{DC1}*=700V,* V_{Batt}*=400V*. A *500Ω* resistor was connected in parallel to *C1* to generate a voltage unbalance. When the voltage equalization is

activated, V_{C1} is quickly made equal to V_{C2}, while the output DC voltage is held constant.

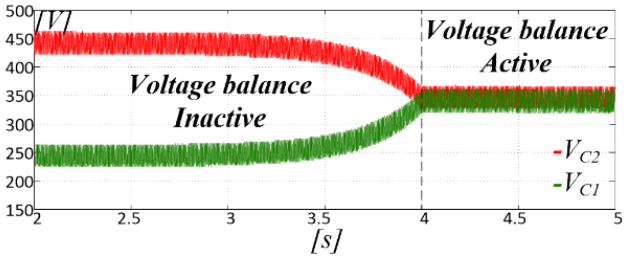


Fig. 4.15 Equalization of 3L T-Type dc-bus capacitors voltage. (w_r=102rad/s, V_{DCX}=700V, V_{DCY}=400V, 80% rated current).

4.2.5 Experimental tests on 4kW prototype.

Experimental validation was carried out on a *4kW* OEW prototype, as illustrated in Fig. 4.16.

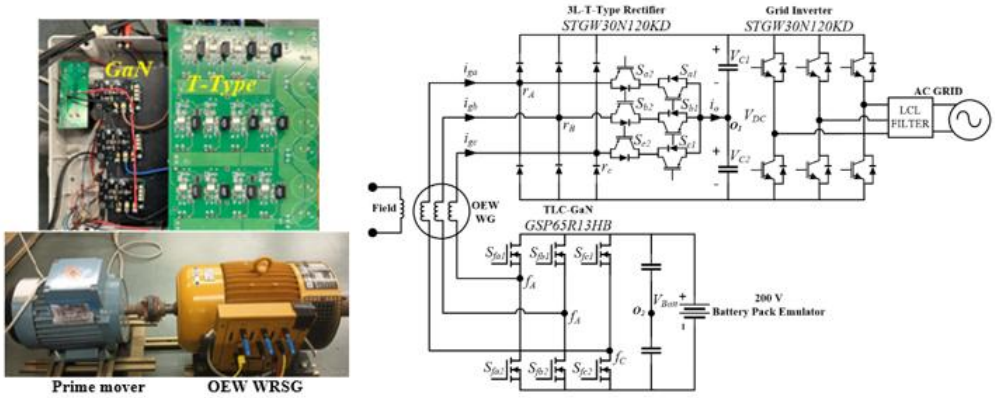


Fig. 4.16 Experimental system and schematic.

It is important to emphasize that the experimental results obtained from the *4kW* prototype remain valid for the *20kW* system. As illustrated in Fig. 4.17, experimental tests were conducted on the proposed system by varying the fundamental frequency and the k_v parameter. It can be observed that efficiency remains high for a k_v factor ranging from 0.31 to 0.5, which demonstrates the versatility of the proposed topology across a broad application range. Indeed, it is possible to scale the system in terms of power and voltage while operating

within the analyzed k_v range. Naturally, an increase in the overall system power would primarily result in a decrease in efficiency due to the proportional increase in power losses. Furthermore, regarding the switching frequency, it is constrained solely by the technological and control limitations of the devices employed in the two-level converter.

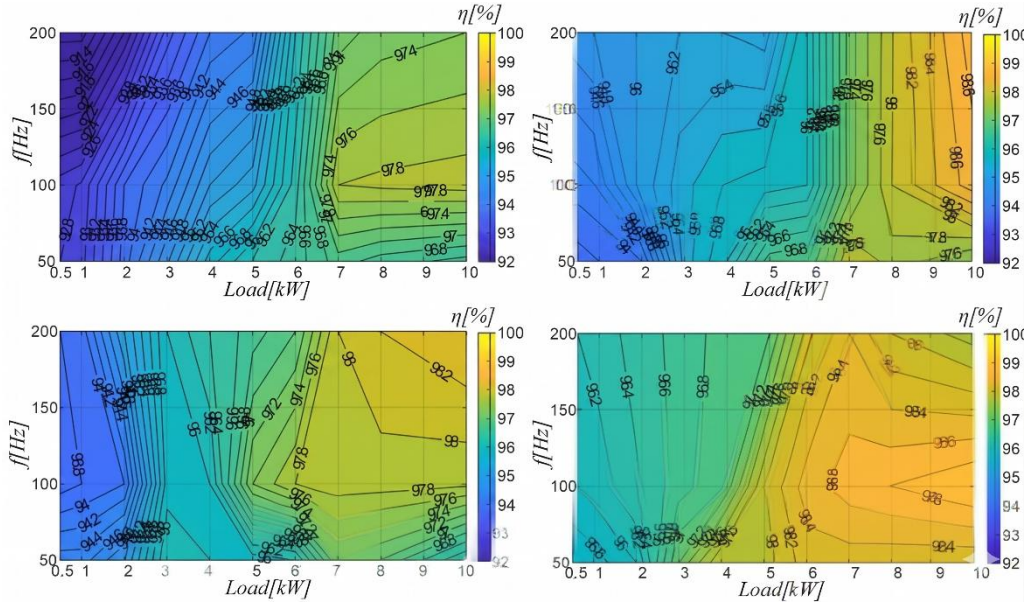


Fig. 4.17 Experimental efficiency of the proposed prototype: (up-left) k_v=0.5; (up-right) k_v=0.4375; (down-left) k_v=0.375; (down-right) k_v=0.3125.

GI is supplied by a *700V* DC bus and delivers a *400V* rms line-to-line AC voltage. The X converter is powered by a *4kW* open-end-winding Wound-Rotor Synchronous Generator (WRSG), whose parameters are given in Tab. 4.6, and the generator itself is mechanically driven by an induction motor. The Y converter is connected to a *400V* battery-pack emulator and operates at *30kHz* using SVPWM strategy. The system employs GaN FETs, Si-IGBTs, and power diodes, with all semiconductor parameters listed in Tab. 4.6. Control of both the X and Y converters is implemented on a dSPACE MicroLabBox 1260 DSP board, enabling precise real-time management of the experimental setup. A 5000ppr encoder provides the angular position of the generator shaft. The effectiveness of the predictive phase-current shaping strategy is illustrated in Fig. 4.18, which compares steady-state operation with and without active filtering and with the closed-loop current control deactivated. To evaluate the

dynamic response of the closed-loop current controller, a step change in the q-axis stator current reference was applied, as shown in Fig. 4.19. The generator phase current promptly increased, accurately reaching the target value of –5 A.

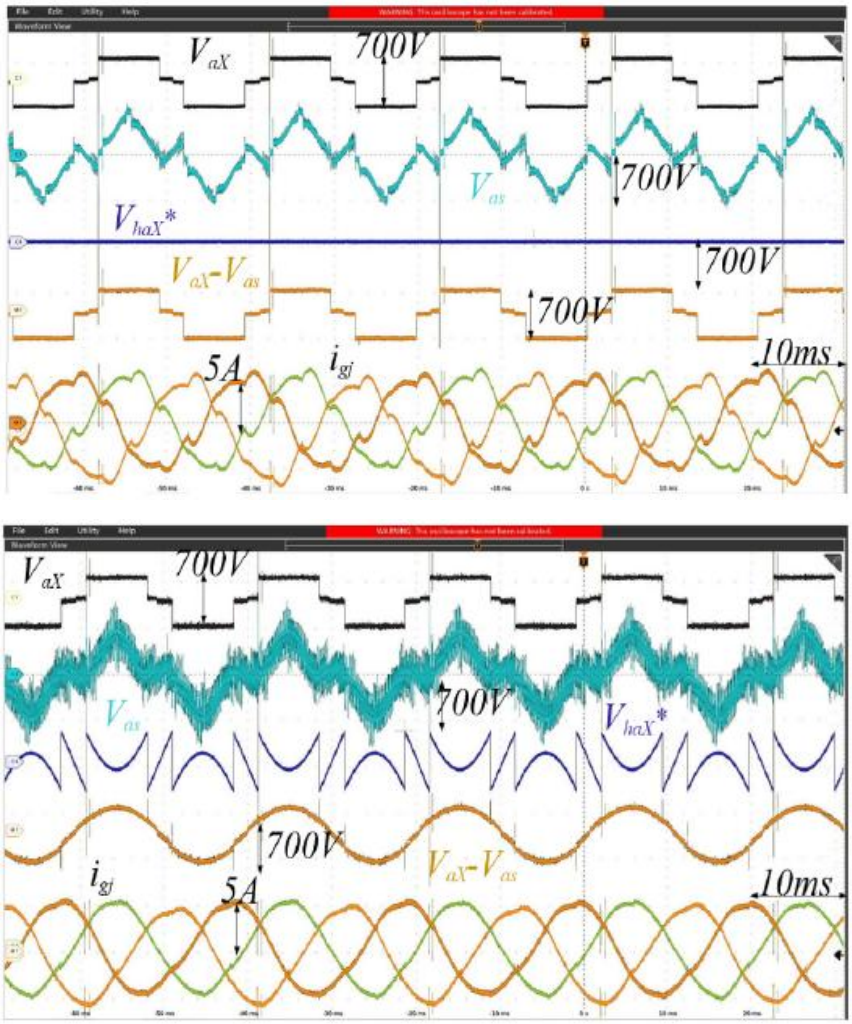


Fig. 4.18 Predictive phase current shaping inactive (up), active (down): V_{aX}, V_{as}, V_{haX}*, V_{aX}-V_{as}, i_{gj}. (w_r=1500rpm, V_{DCX}=700V, V_{DCY}=400V).

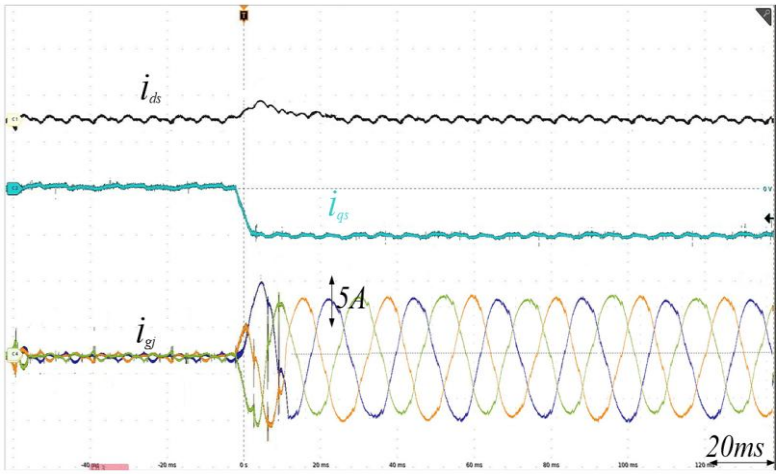
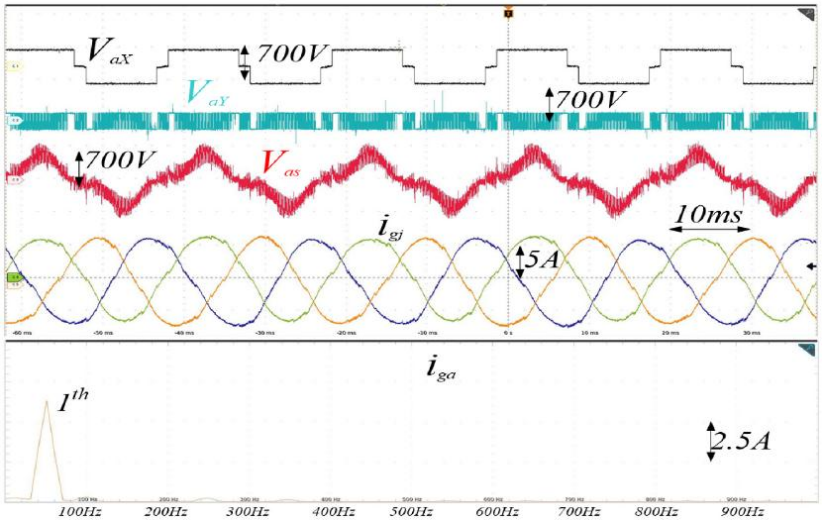
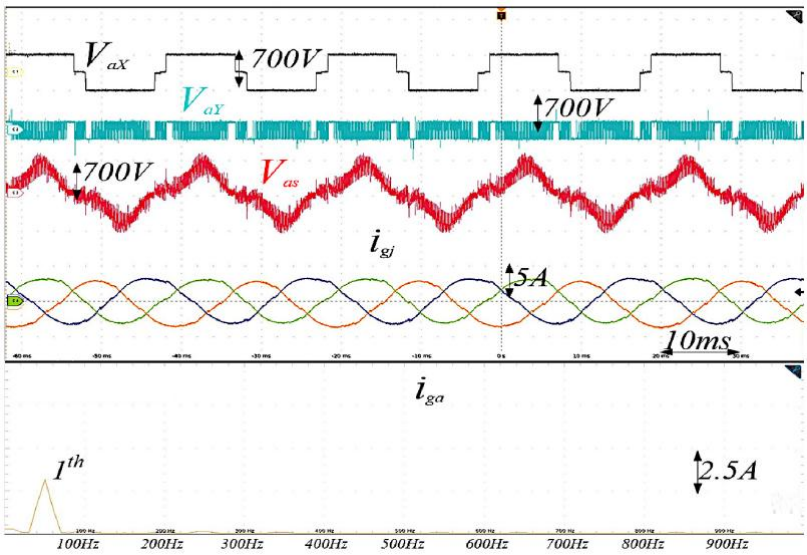


Fig. 4.19 Step variation of the q axis component of the stator current reference from 0 to -5A.

Figure 4.20 presents the main electrical quantities recorded during operation at 90%, 50%, and 10% of rated load, with V_{DCX}=*700V*, V_{DCY}=*400V* and ω_r=*157* rad/s, (corresponding to *50Hz*). Across the entire load range, the generator phase current i_{gj} remains nearly sinusoidal, and the system achieves a consistently low THD, as shown in Fig. 4.21.



(a)



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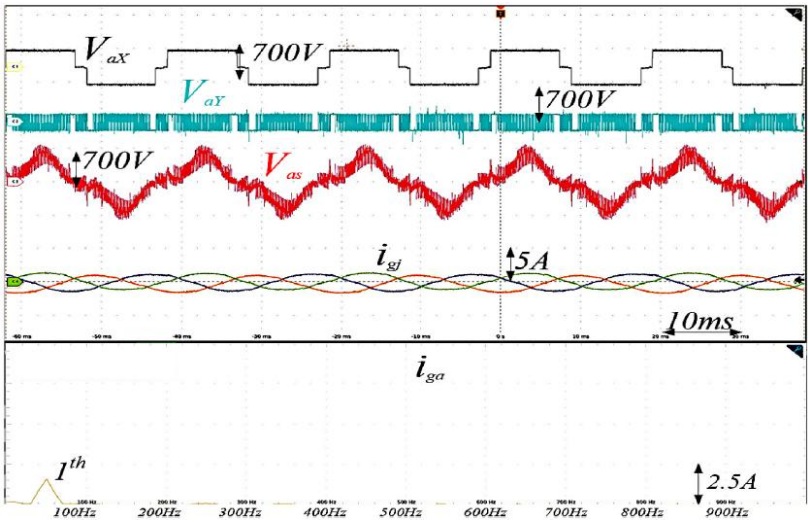


(c)

Fig. 4.20 V_{aX}, V_{aY}, V_{as}, i_{gj}, i_{ga} frequency spectrum. (w_r=1500rpm, V_{DCX}=700V, V_{DCY}=400V); (a) 90% power; (b) 50% power; (c) 10% power.

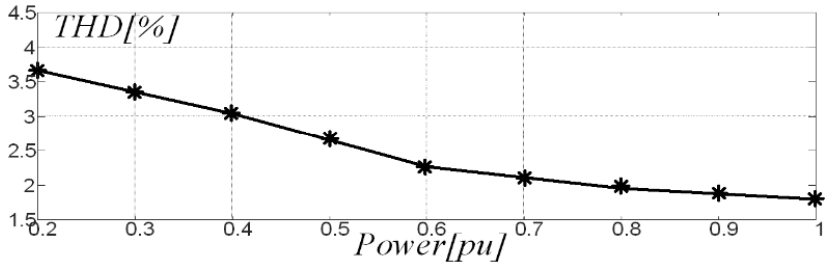


Fig. 4.21 THD of generator current iga vs. power. (w_r = 1500rpm, V_{DCX} = 700V, V_{DCY} = 400V).

Finally, the case of zero rotor speed is considered in Fig. 4.22, where the power demanded by the AC grid is entirely supplied by the battery.

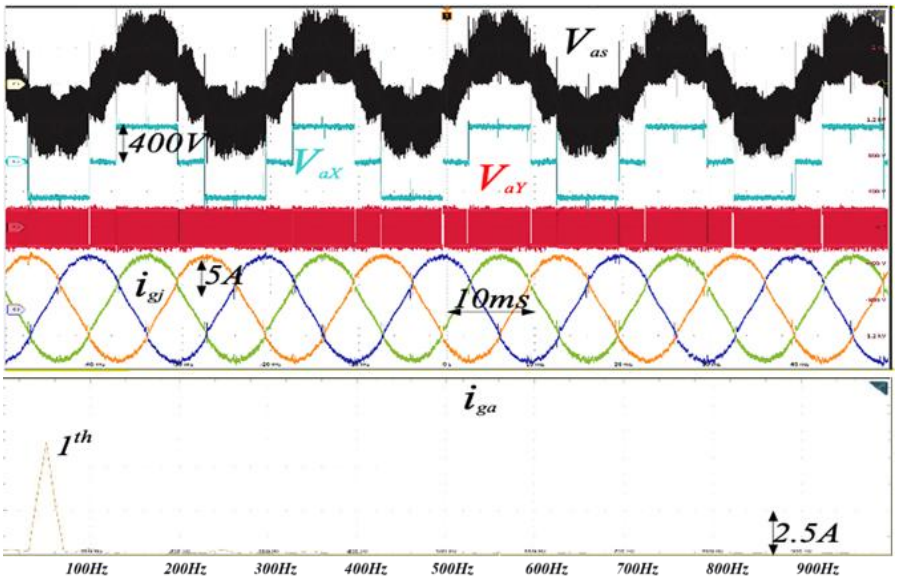


Fig. 4.22 Inactive AC generator, 90 % power: V_{aX}, V_{aY}, V_{as}, i_{gj}, i_{ga} frequency spectrum. (w_r = 0rpm, V_{DCX} = 700V, V_{DCY} = 400V).

Table 4.6 Parameters of OEW prototype.

X Converter (3L T-Type rectifier)		**Grid Inverter**	
Rated power	4kW	Rated power	4kW
Input AC voltage (line to line rms)	400 V	Input DC voltage	700V
Output DC voltage	700V	Output AC voltage	400V (3f, RMS)
DC Link Capacitors	2 x 860μF 500V	Si-IGBT	4 x STGW30N60KD 600 V, 30 A
Switching frequency	0-60Hz	Switching frequency	30kHz
Si-IGBT	6 x STGW30N60KD 600V, 30A	**Wound Rotor Synchronous Generator**	
Clamping diodes	6 x RURG80100, 1000V, 80A	Rated power	4kW
Y Converter Converter (2L inverter)		Rated voltage (line to line rms)	400V
Rated power and voltage	4kW	Rated speed	157rad/s
Input DC voltage	400V	Pole pairs	2
Output AC voltage (line to line rms)	245V	Stator inductance	40mH
DC Link Capacitor	860μF 500V	Stator resistance	9Ω
Switching frequency	30kHz	**AC Three-Phase Grid**	
GaN FET	6 GaN GSP65R13HB, 650V, 47A	Rated voltage	400V rms
Voltage harmonics eliminated	5^{th}, up to 51^{th}	Frequency	50Hz

4.3 EXPERIMENTAL ANALYSIS.

The efficiency, power quality, and CMV levels achieved with the proposed OEW structure were compared against those obtained with alternative topologies, namely the C-DC-Bus (Fig. 4.2a), C-AC-Link (Fig. 4.2b), Dual Inverter Grid (Fig. 4.3a), and 3L-OEW-Generator (Fig. 4.3b) configurations. The comparison was experimentally carried out using converter prototypes with identical power ratings. Table 4.7 summarizes the parameters of all the systems considered.

Table 4.7 Parameters of competitor configurations.

C-DC-Bus Configuration		
TLC PWM Rectifier	Rated power and voltage	4kW, 700V
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 x STGW30N120KD, 1200V, 30A
Bidirectional DC/DC	Rated power and voltage	4kW, 800V
	Configuration	Full-Bridge
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	4 x STGW30N120KD, 1200V, 30A
C-AC-Link Configuration		
Controlled Rectifier and Battery Inverter	Rated ower and voltage	4kW, 700V
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 x STGW30N120KD, 1200V, 30A
Dual-Grid Inverter Configuration		
Controlled Rectifier	Rated power and voltage	4kW, 700V
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	0-50Hz
	Diodes	6 xe RURG80100, 1000V,80A
DC/DC Boost	Rated power and voltage	4 kW, 800V
	Inductance	5mH
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	STGW30N120KD, 1200V, 30A
Battery Inverter	Rated power and voltage	4 kW, 400V
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 x STGW30N60KD, 600 V, 30 A
AC Three-Phase Transformer	Rated power and voltage	4 kVA, 400 V/ 400 V, OEW
	Iron loss	25W
	Copper loss	75W
3L-OW-Generator Configuration		
Controlled Rectifier	Rated power and voltage	4 kW, 700 V
	DC Link Capacitor	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 x STGW30N120KD, 1200 V,30 A
Battery Inverter	Rated power and voltage	4 kW, 400 V
	DC Link Capacitors	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 IGBT STGW30N60KD, 600V,30A

In the C-DC-Bus configuration, the controlled rectifier is implemented using six Si-IGBTs identical to those employed in the proposed OEW topology. The bidirectional DC-DC converter, operating at *800V*, uses six *1200V Si-IGBTs*, while the battery voltage is set to *800V*. Both converters operate at a switching frequency of *30kHz*.

In the C-AC-Link configuration, both the controlled rectifier and the battery inverter operate at *30kHz*, each employing six *1200V* Si-IGBTs, given the *800V* DC link voltage.

For the Dual Inverter Grid configuration, the uncontrolled rectifier utilizes six *1200V* diodes, while the DC-DC boost converter employs a single *1200V* Si-IGBT. As reported in [24], the battery-side converter operates at approximately half the output voltage of the DC-DC boost converter, corresponding to *400V*, and is implemented with six *650V* Si-IGBTs. This configuration also requires a *6kVA*, *400/400V* transformer, whose primary winding is arranged in an OEW configuration.

Finally, the 3L-OEW-Generator topology uses six *1200V* Si-IGBTs in the controlled rectifier and six *650V* Si-IGBTs in the battery inverter, as in the previous case where the voltage ratio $k_v = 0.5$. All Si-IGBTs operate at a switching frequency of *30kHz*, and all configurations employ the same WRSG described in Table 4.5. The Grid Interface is identical for all cases, with parameters listed in Table 4.8. The GI is connected to the grid through an LCL filter with $L = 120\ \mu H$ and $C = 10\ \mu F$.

Table 4.8 Parameters of Grid Inverter used for all configurations under test.

Grid Inverter		
Controlled Rectifier	Rated power and voltage	4 kW, 700 V
	DC Link Capacitors	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 x STGW30N120KD, 1200 V, 30A
Battery Inverter	Rated power and voltage	4 kW, 400 V
	DC Link Capacitors	2 x 860µF, 500V
	Switching frequency	30kHz
	SI-IGBT	6 x STGW30N60KD, 600 V, 30 A

4.3.1 Efficiency analysis.

The efficiency of each converter was evaluated for all configurations as a function of rotor speed and output power, as illustrated in Fig. 4.23. This assessment was carried out by measuring both input and output power across the entire operating range. Among all the investigated configurations, the TLC-GaN and the 3L T-Type converters achieved the highest efficiency levels. The superior performance of the TLC-GaN converter is attributed to the use of GaN-FETs, characterized by their very low on-state resistance and fast switching transitions (rise and fall times). Conversely, the high efficiency of the 3L T-Type inverter results from its nearly negligible switching losses, enabled by operation at a relatively low switching frequency. In contrast, the efficiency of the DC/DC PWM converter remains essentially independent of the rotor speed.

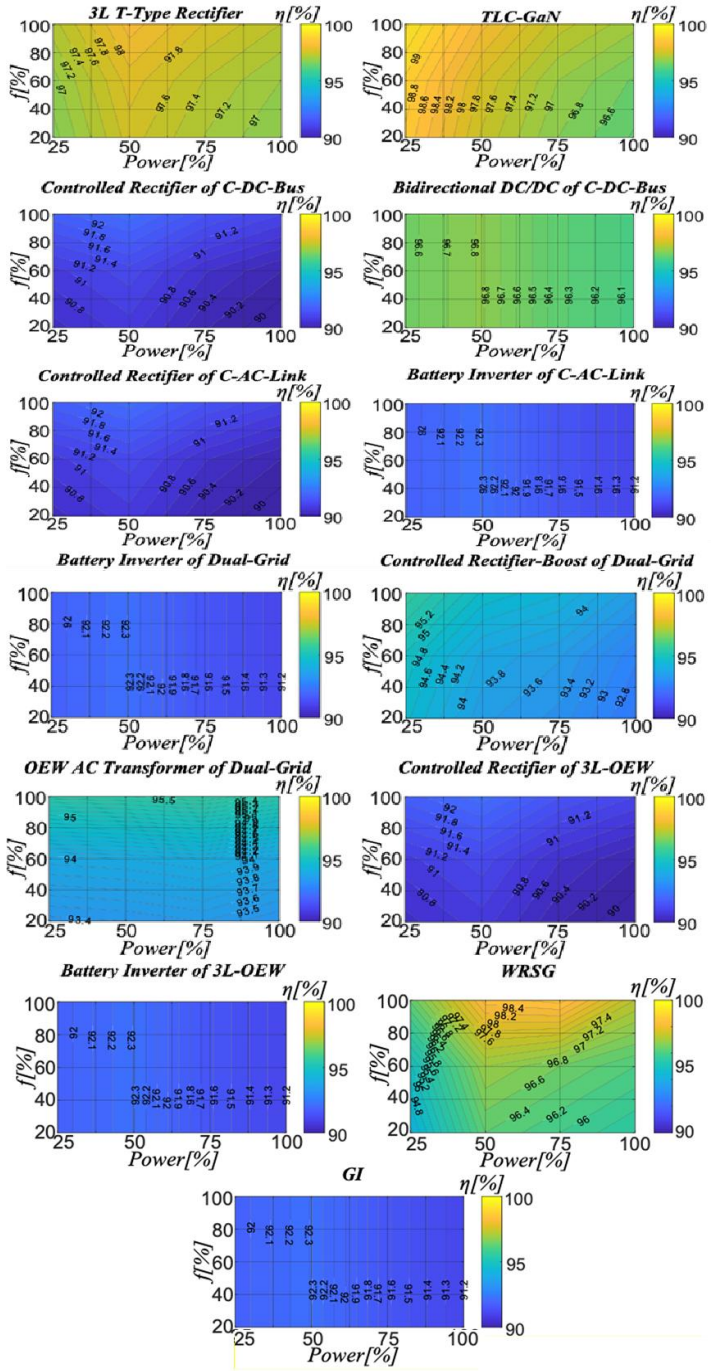


Fig. 4.23 Efficiency of all components vs. power and speed.

4.3.2 WG to grid power efficiency.

In all the configurations considered, the power flow from the generator to the grid passes through the Controlled Rectifier, the DC Bus, and the GI. In the C-DC-Bus, C-AC-Link, and 3L-OEW-Generator configurations, the power path includes the Controlled PWM Rectifier, the DC Bus, and the PWM-based GI. Conversely, in the Dual Inverter Grid configuration, the power flows through the Controlled PWM Rectifier, the DC Bus, the PWM-GI, and the OEW AC Transformer. In the proposed OEW system, power transfer occurs through the 3L T-Type Rectifier, the DC Bus, and the PWM-GI. As illustrated in Fig. 4.24, the proposed OEW configuration achieves the highest overall efficiency, primarily due to the reduced switching losses associated with the 3L T-Type rectifier. In contrast, the Dual Inverter Grid configuration exhibits lower efficiency, mainly because of the additional power losses introduced by the OEW AC Transformer.

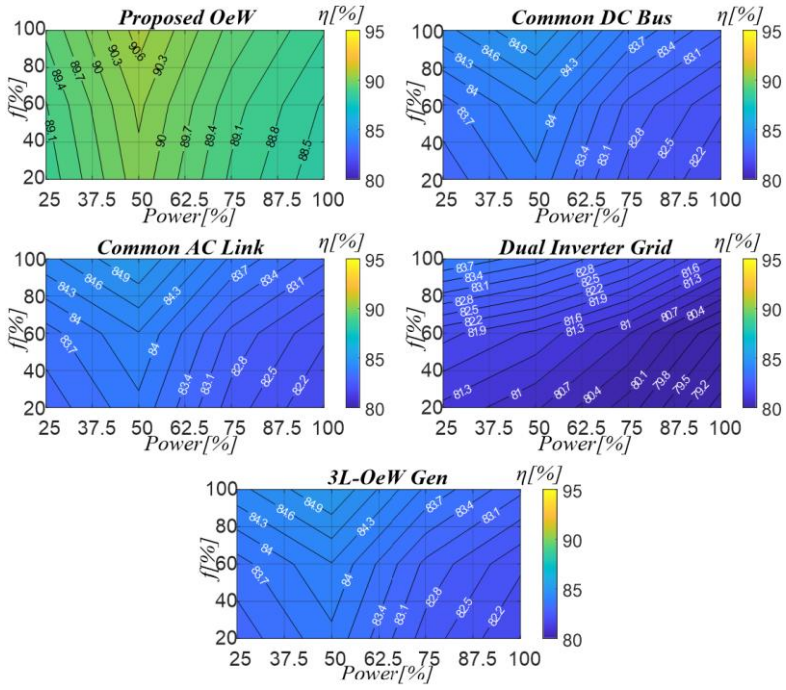


Fig. 4.24 Generator to grid power transfer efficiency.

4.3.3 WG to battery power efficiency.

The power transfer from the generator to the battery follows different paths depending on the specific configuration. In the C-DC-Bus configuration, the power flows through the Controlled PWM Rectifier and the bidirectional DC/DC converter. In the C-AC-Link configuration, the path is longer, including the Controlled PWM Rectifier, the PWM-GI, and the Battery Inverter/Rectifier. The 3L-OEW-Generator and the proposed OEW configuration feature shorter transfer paths, involving only the Battery Inverter/Rectifier and the TLC-GaN stage, respectively. As illustrated in Fig. 4.25, the proposed OEW configuration achieves the highest efficiency, primarily due to the low power losses associated with the TLC-based GaN devices.

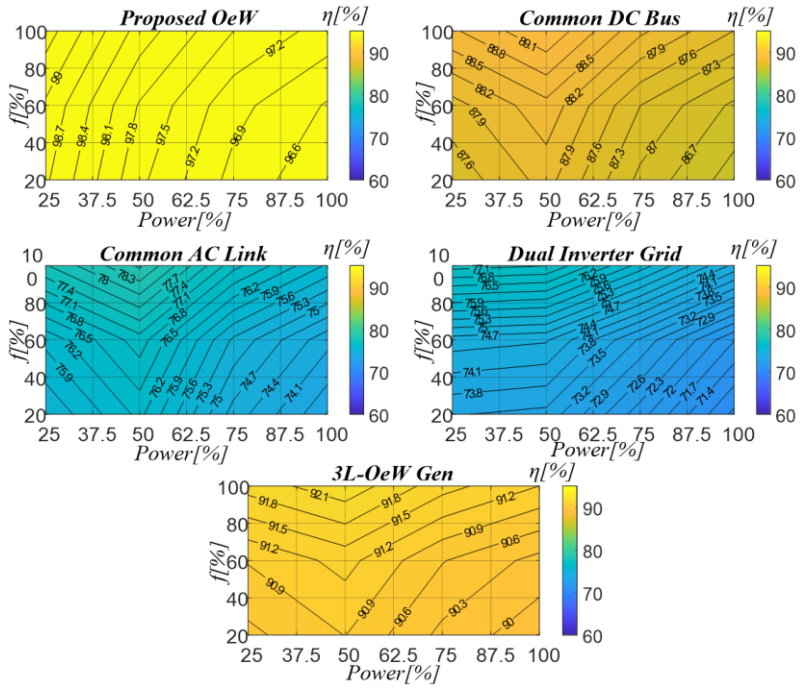


Fig. 4.25 Generator to battery to grid power transfer efficiency.

4.3.4 Battery to grid power efficiency.

In the C-AC-Link configuration, the power supplied by the battery to the grid follows a very short path, comprising only the PWM-GI or Controlled PWM Rectifier. Longer paths are taken in the C-DC-Bus, Dual Inverter Grid, and

proposed OEW configuration. Figure 4.26 shows that the proposed OEW configuration exhibits the lowest efficiency excepting the 3L-OW-Generator.

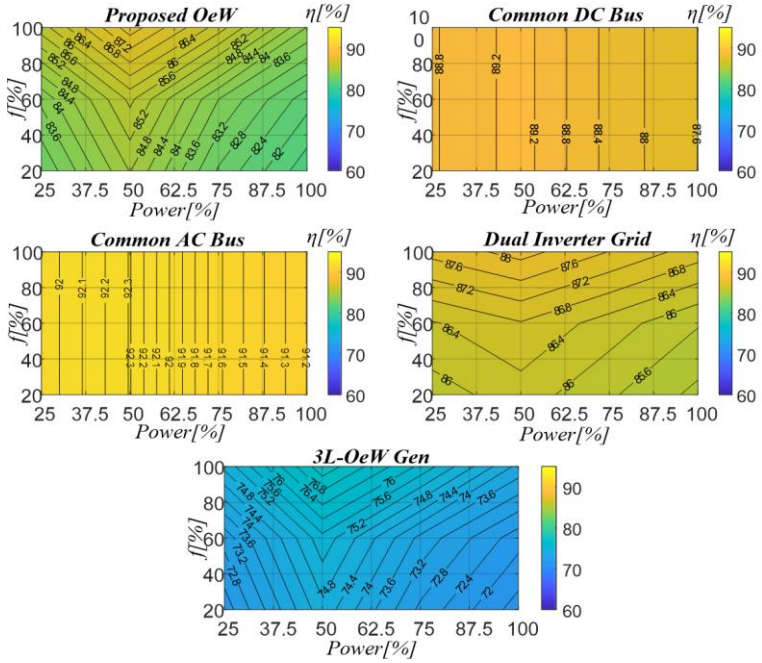


Fig. 4.26 Battery to grid power transfer efficiency.

4.3.5 Average efficiency comparison.

A comparative evaluation of the configurations considered is presented in the average-efficiency radar chart shown in Fig. 4.28, for load levels corresponding to 100%, 50%, and 25% of the rated load frequency. The proposed OEW structure demonstrates superior efficiency in WG-to-Battery, WG-to-Grid, and overall cycle efficiency paths. This improvement is partly attributed to the shorter power transfer path between the wind generator and the battery, and partly to the high efficiency of the TLC-GaN inverter.

In the WG-to-Grid power path, all configurations include the same conversion stages, a controlled rectifier and the GI. The observed performance difference, as shown in Fig. 4.23, stems from the higher efficiency of the 3L T-Type inverter used in the proposed OEW structure. This is achieved by operating the converter at the fundamental frequency, which nearly eliminates switching losses. Moreover, the Si-IGBTs forming the three bidirectional switches of the

3L T-Type inverter are subjected to only half the DC-link voltage ($V_{DCX}/2$), further reducing conduction and switching losses compared to other configurations.

The best efficiency in the Battery-to-Grid path is achieved by the C-AC-Link configuration, as it requires only a single power converter to interface the battery with the grid. However, it should be noted that for battery voltages around *400V*, as in the proposed structure, the C-AC-Link configuration would necessitate an additional DC-DC boost converter to raise the voltage to *700–800V*. This step is essential for the battery inverter to operate and deliver power to the grid but would negatively impact the overall Battery-to-Grid efficiency.

As a result, the proposed OEW structure achieves the highest overall cycle efficiency in the WG–Battery–Grid power path, as shown in fig. 4.27 which is a key advantage for wind generation systems integrated with energy storage.

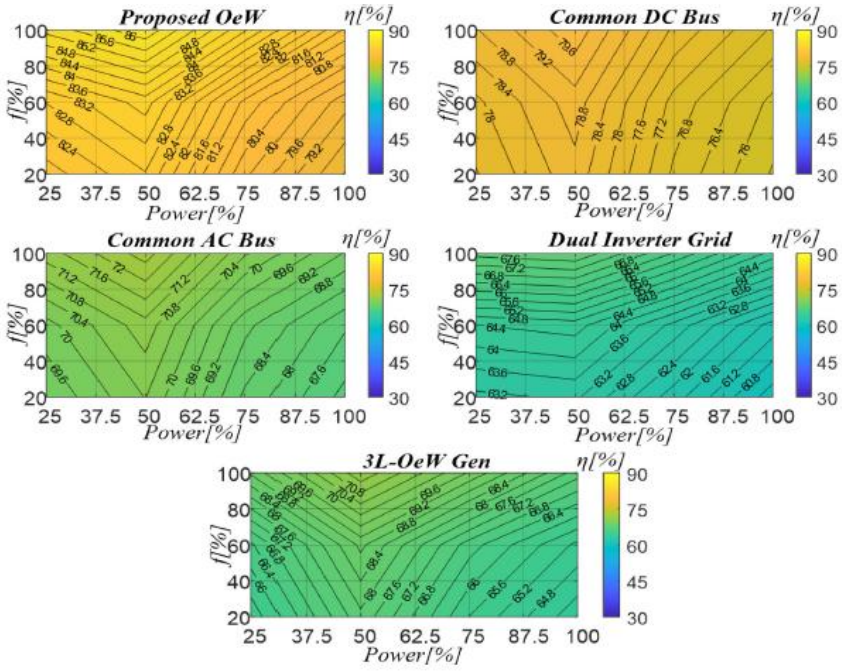


Fig. 4.27 Cycle power transfer efficiency.

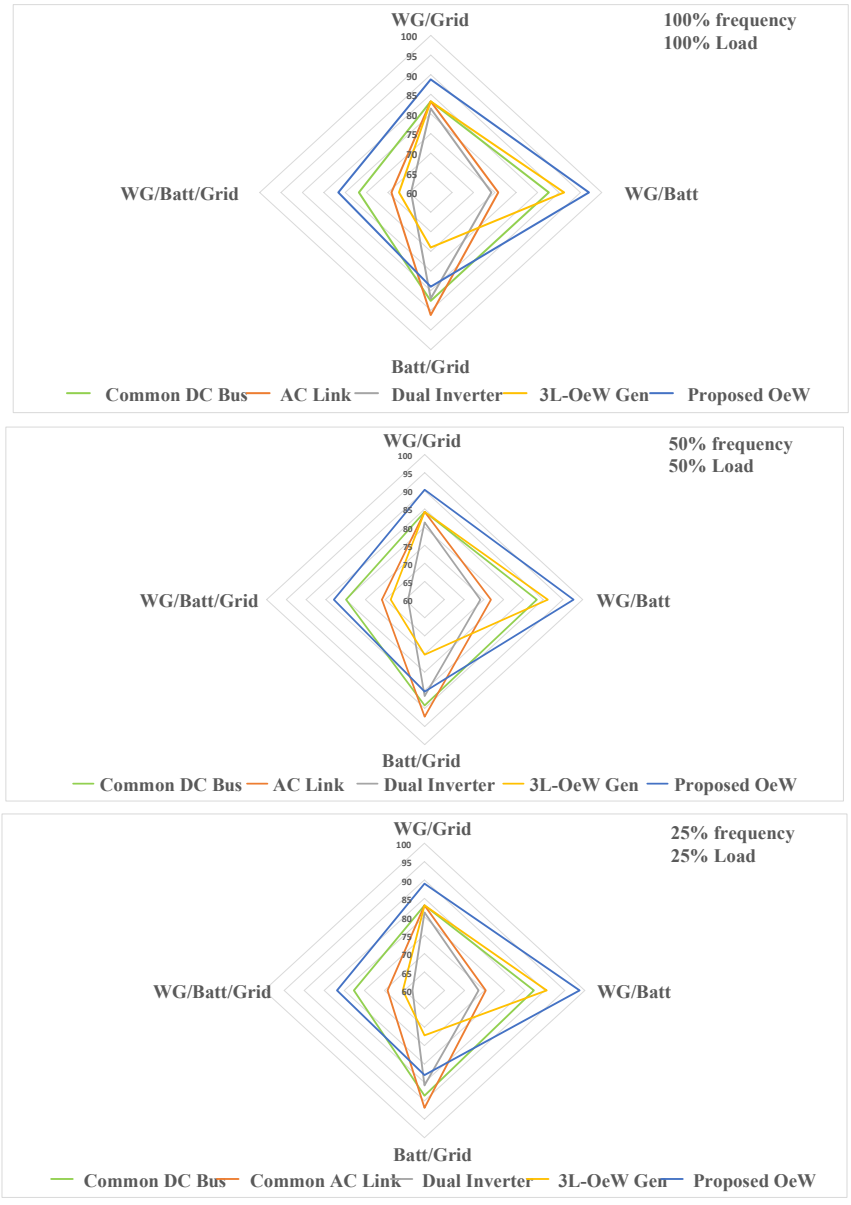


Fig. 4.28 Average efficiency comparison at 100% Load-frequency, 50% Load-frequency and 25% Load-frequency.

4.3.6 CMV and Total Harmonic Distortion (THD) analysis.

Common-Mode Voltage (CMV) in drive systems refers to the voltage difference between the machine's neutral point (or ground) and the reference point of the drive, typically the DC bus of the power converter. In motor drive applications, CMV represents a critical design concern, as it can adversely affect both the performance and reliability of the system.

During power device switching events, high-frequency voltage spikes and switching noise are generated, which induce CMV between the machine windings and the system ground. This phenomenon can lead to several detrimental effects, including increased stress on machine insulation, EMI, and bearing degradation due to circulating currents induced by CMV.

A well-established approach to mitigating CMV is the adoption of MLC topologies. By increasing the number of voltage levels (N_L), MLCs effectively reduce the voltage change rate (dV/dt) and produce a smoother output voltage waveform. This smoother waveform results in lower CMV magnitude and reduced high-frequency content, thereby mitigating insulation stress, minimizing EMI emissions, and preventing bearing damage.

The CMV for an OEW structure can be expressed as [29]:

$$V_o = \frac{1}{6}(V_{aX} + V_{bX} + V_{cX} + V_{aY} + V_{bY} + V_{cY}) \quad (\mathbf{19})$$

Table 4.9 CMV, THD_v and Efficiency comparison.

Top	N_L	CMV level	CMV_{pk}	Peak value of cycle efficiency and THD_v					
				100%Load 100%f		50%Load 100%f		25%Load100 %f	
				η [%]	THDv [%]	η [%]	THDv [%]	η [%]	THDv [%]
C-DC-Bus	2	$\pm V_{DC}/2$ $\pm V_{DC}/6$	$V_{DC}/2$	76.8	19.5	79.6	19.8	78.8	20.5
C-AC-Link	2	$\pm V_{DC}/2$ $\pm V_{DC}/6$	$V_{DC}/2$	69.2	19.3	72	19.5	71.6	20.3
Dual-Grid Inv	2	$\pm V_{DC}/2$ $\pm V_{DC}/6$	$V_{DC}/2$	64.4	18.9	67.6	18.9	67.6	19.9
3L-OW-Gen	4	$\pm V_{DC}/2$ $\pm V_{DC}/3$ $\pm V_{DC}/6$	$V_{DC}/2$	67.2	9.9	70.8	9.9	68.8	10.9
Prop OEW	6	$\pm V_{DC}/3$ $\pm V_{DC}/4$ $\pm V_{DC}/12$	$V_{DC}/3$	81.6	4.4	86	5.3	86.2	6

According to Tab. 4.1 and 4.6, since $k_v=0.57$, the proposed OEW structure operates as a 6-Level voltage converter. When analyzing the CMV in the various structures, it is evident that the proposed OEW structure generates the lowest CMV, with a peak value equal to $V_{DC}/3$, as shown in Table 4.9. Regarding power quality, the Total Harmonic Distortion of the generator phase voltage V_{js} (THD_v) was measured at 25%, 50%, and 100% load. The THD_v was measured considering voltage harmonics up to the 90^{th} order. As shown in Tab. 4.9, the proposed OEW structure generates the lowest THD due to the higher number of voltage levels compared to the other topologies, an aspect also demonstrated in [17].

4.4 CONCLUSIONS.

A high-efficiency three-port power conversion system for wind generators with integrated energy storage has been developed. The system adopts a hybrid Si/GaN approach, implemented in an OEW configuration. This design optimizes the power flow among system components, achieving an average efficiency comparable to that of a fully GaN-based three-port converter. Notably, this performance is obtained while employing only six GaN switches, each operating at less than half the rated voltage of the main DC bus. The system exhibits an

extensive operating range dictated by the technological constraints of the power devices.

Experimental results demonstrate that the proposed system outperforms competing topologies in several key aspects, including average cycle efficiency (+7.4% at 25% load, +6.4% at 50% load, and +4.8% at 100% load compared to the best-performing alternative), common-mode voltage (reduced from $V_{DC}/2$to $V_{DC}/3$), and total harmonic distortion (−4.9% at 25% load, −4.67% at 50% load, and −5.5% at 100% load relative to the best alternative topology).

The superior efficiency is primarily attributed to the nearly zero switching losses of the 3L T-Type rectifier, which operates at fundamental frequency, in combination with the low switching and conduction losses of the GaN-based TLC inverter. In particular, the wind generator–to–battery power transfer efficiency reaches a peak value of 99%. The reduced THDv results from the increased number of voltage levels per switch (N_{LS}=0.33) achieved by the proposed system, compared to other configurations (N_{LS}=0.125 for the C-DC-Bus, 0.111 for the Dual-Grid Inverter, and 0.22 for the 3L-OEW Generator). The high switching frequency of the GaN devices further contributes to waveform quality improvement. Moreover, the reduced common-mode voltage positively impacts generator bearing lifetime by mitigating insulation stress and circulating current effects.

4.5 REFERENCE LIST.

[1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu and S. Jain, "Multilevel Inverter Topologies With Reduced Device Count: A Review," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135-151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012;

[2] Kotb B. Tawfiq, Arafa S. Mansour, Haitham S. Ramadan, Mohamed Becherif, E.E. El-kholy, "Wind Energy Conversion System Topologies and Converters: Comparative Review," Energy Procedia, Volume 162, 2019, Pages 38-47, ISSN 1876-6102, https://doi.org/10.1016/j.egypro.2019.04.005;

[3] Amano, R. S. (September 11, 2017). "Review of Wind Turbine Research in 21st Century." ASME. *J. Energy Resour. Technol*. September 2017; 139(5): 050801. https://doi.org/10.1115/1.4037757;

[4] Global wind report 2016-Annual market update, Global Wind Energy Council, 2017;

[5] Francisco Díaz-González, Andreas Sumper, Oriol Gomis-Bellmunt, Roberto Villafáfila-Robles, "A review of energy storage technologies for wind power applications," Renewable and Sustainable Energy Reviews, Volume 16, Issue 4, 2012, Pages 2154-2171, ISSN 1364-0321, https://doi.org/10.1016/j.rser.2012.01.029;

[6] A. Merabet, K. Tawfique Ahmed, H. Ibrahim, R. Beguenane and A. M. Y. M. Ghias, "Energy Management and Control System for Laboratory Scale Microgrid Based Wind-PV-Battery," in *IEEE Transactions on Sustainable Energy*, vol. 8, no. 1, pp. 145-154, Jan. 2017, doi: 10.1109/TSTE.2016.2587828;

[7] A. Sattar, A. Al-Durra, C. Caruana, M. Debouza and S. M. Muyeen, "Testing the Performance of Battery Energy Storage in a Wind Energy Conversion System," in *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 3196-3206, May-June 2020, doi: 10.1109/TIA.2020.2979792;

[8] Barelli, Linda, Dario Pelosi, Dana Alexandra Ciupageanu, Panfilo Andrea Ottaviano, Michela Longo, and Dario Zaninelli. 2021. "HESS in a Wind Turbine Generator: Assessment of Electric Performances at Point of Common Coupling with the Grid" *Journal of Marine Science and Engineering* 9, no. 12: 1413. https://doi.org/10.3390/jmse9121413;

[9] Piotr Gajewski & Krzysztof Pieńkowski, 2021. "Control of the Hybrid Renewable Energy System with Wind Turbine, Photovoltaic Panels and Battery Energy Storage," Energies, MDPI, vol. 14(6), pages 1-23, March.

[10] M. M. Gulzar, A. Iqbal, D. Sibtain and M. Khalid, "An Innovative Converterless Solar PV Control Strategy for a Grid Connected Hybrid PV/Wind/Fuel-Cell System Coupled With Battery Energy Storage," in *IEEE Access*, vol. 11, pp. 23245-23259, 2023, doi: 10.1109/ACCESS.2023.3252891;

[11] H. Zhang, W. Xiang and J. Wen, "Dual Grid-Forming Control With Energy Regulation Capability of MMC-HVDC System Integrating Offshore Wind Farms and Weak Grids," in *IEEE Transactions on Power Systems*, vol. 39, no. 1, pp. 261-272, Jan. 2024, doi: 10.1109/TPWRS.2023.3244807;

[12] R. Wu, J. A. Ortiz-Gonzalez and A. Alatise, "A Case Study of Power Electronics in Wind Energy Conversion," *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, Online Conference, 2020, pp. 349-354, doi: 10.1049/icp.2021.1107.

[13] K. Lee, H. Shin and J. Choi, "Comparative analysis of power losses for 3-Level NPC and T-type inverter modules," *2015 IEEE International Telecommunications Energy Conference*

(INTELEC), Osaka, Japan, 2015, pp. 1-6, doi: 10.1109/INTLEC.2015.7572357.

[14] A. Bakbak *et al*., "PMSG-Based Dual-Port Wind-Energy Conversion System With Reduced Converter Size," in *IEEE Access*, vol. 9, pp. 118953-118967, 2021, doi: 10.1109/ACCESS.2021.3107595;

[15] G. Baia, S. De Caro, S. Foti, H. H. Khan and A. Testa, "Efficiency Assessment of an Open-End Winding Inverter Exploiting a Mixed Si/GaN Technology," *2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe)*, Aalborg, Denmark, 2023, pp. 1-9, doi: 10.23919/EPE23ECCEEurope58414.2023.10264533.

[16] Salvatore Foti, Antonio Testa, Gioele Baia, Haseeb Hassan Khan, Danilo Campagna, “A high efficiency three-port power converter for wind generators with energy storage,” Journal of Energy Storage, Volume 116, 2025, 116029, ISSN 2352-152X, https://doi.org/10.1016/j.est.2025.116029;

[17] M. Pathmanathan and P. W. Lehn, "Control Algorithm for Energy Storage Integration with an Open-Winding Wind Turbine Generator," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Toronto, ON, Canada, 2021, pp. 1-6, doi: 10.1109/IECON48115.2021.9589343;

[18] H. Abu-Rub, J. Holtz, J. Rodriguez and G. Baoming, "Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596, Aug. 2010, doi: 10.1109/TIE.2010.2043039;

[19] M. Vijeh, M. Rezanejad, E. Samadaei and K. Bertilsson, "A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9479-9502, Oct. 2019, doi: 10.1109/TPEL.2018.2890649;

[20] A. Yazdani and R. Iravani, "A neutral-point clamped converter system for direct-drive variable-speed wind power unit," in *IEEE Transactions on Energy Conversion*, vol. 21, no. 2, pp. 596-607, June 2006, doi: 10.1109/TEC.2005.860392;

[21] Y. Zhang, X. Peng, X. Yuan, Y. Li and K. Wang, "A Unidirectional Cascaded High-Power Wind Converter With Reduced Number of Active Devices," in *IEEE Access*, vol. 11, pp. 10902-10911, 2023, doi: 10.1109/ACCESS.2023.3238870;

[22] J. -S. Lee and K. -B. Lee, "Open-Switch Fault Tolerance Control for a Three-Level NPC/T-Type Rectifier in Wind Turbine Systems," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 1012-1021, Feb. 2015, doi: 10.1109/TIE.2014.2347912;

[23] V. T. Somasekhar, M. R. Baiju, K. K. Mohapatra and K. Gopakumar, "A multilevel inverter system for an induction motor with open-end windings," *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*, Seville, Spain, 2002, pp. 973-978 vol.2, doi: 10.1109/IECON.2002.1185404;

[24] S. D. G. Jayasinghe, D. M. Vilathgamuwa and U. K. Madawala, "A dual inverter based supercapacitor direct integration scheme for wind energy conversion systems," *2010 IEEE International Conference on Sustainable Energy Technologies (ICSET)*, Kandy, Sri Lanka, 2010, pp. 1-6, doi: 10.1109/ICSET.2010.5684459;

[25] S. Foti *et al.*, "An Optimal Current Control Strategy for Asymmetrical Hybrid Multilevel Inverters," in *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4425-4436, Sept.-Oct. 2018, doi: 10.1109/TIA.2018.2832024;

[26] S. Foti, A. Testa, G. Scelba, V. Sabatini, A. Lidozzi and L. Solero, "A Low THD Three-Level Rectifier For Gen-Set Applications," in *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6150-6160, Nov.-Dec. 2019, doi: 10.1109/TIA.2019.2937054;

[27] A. Testa, S. Foti, S. De Caro, L. D. Tornello, G. Scelba and G. Scarcella, "Optimal Selection of the Voltage Modulation Strategy for an Open Winding Multilevel Inverter," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 2231-2237, doi: 10.1109/ECCE44975.2020.9235955;

[28] S. Foti, A. Testa, R. Testa, O. Giordano and G. Baia, "An Open-End Winding Wind Generator with Integrated Energy Storage," *2023 International Conference on Clean Electrical Power (ICCEP)*, Terrasini, Italy, 2023, pp. 260-266, doi: 10.1109/ICCEP57914.2023.10247441;

[29] W. Hu, C. Ruan, H. Nian and D. Sun, "Zero-Sequence Current Suppression Strategy With Common-Mode Voltage Control for Open-End Winding PMSM Drives With Common DC Bus," in *IEEE Transactions on Industrial Electronics*, vol. 68, no. 6, pp. 4691-4702, June 2021, doi: 10.1109/TIE.2020.2988221.

CHAPTER 5

Hybrid OEW inverter for electric vehicles.

This chapter is extensively based on the following publication:

G. Baia et al., "Efficiency Assessment of an Open-End Winding Inverter Exploiting a Mixed Si/GaN Technology," 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe), Aalborg, Denmark, 2023, pp. 1-9, doi: 10.23919/EPE23ECCEEurope58414.2023.10264533.

G. Baia et al., "Design and Development of a Mixed Si-GaN Open-End Winding Inverter for Electric Vehicles," in IEEE Transactions on Transportation Electrification, vol. 12, no. 1, pp. 1942-1954, Feb. 2026, doi: 10.1109/TTE.2025.3636205.

5 HYBRID OEW INVERTER FOR ELECTRIC VEHICLES.

5.1 INTRODUCTION

Next-generation electric vehicles (EVs) are transitioning from *400V* to *800V* battery systems to reduce charging times and enhance drivetrain compactness and efficienc [1-3]. However, as discussed in Chapter 2, this voltage increases challenges for traditional Si-IGBT and WBG technologies [4-7]. MLI topologies offer a promising solution by fractioning the total DC-link voltage, thereby enabling the use of high-performance WBG devices, such as *650V*-rated GaN semiconductors [8-11]. Among these, OEW configuration is particularly advantageous over conventional MLI thanks to their lower number of devices per voltage level; improved redundancy, better efficiency and enhanced speed range [12-16], as detailed in Chapter 3. These systems can also be classified as symmetrical when both inverters are supplied with DC bus voltages of equal magnitude [17], or asymmetrical if not [18]. The asymmetrical hybrid multilevel inverter (AHMLI). configuration is shown schematically in Fig. 5.1.

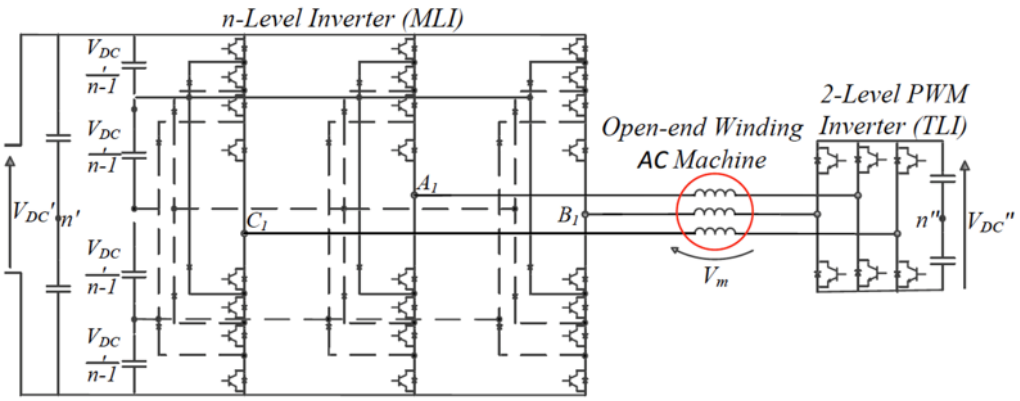


Fig. 5.1 AHMLI configuration.

This structure makes it possible to adopt a mixed Si-IGBT/GaN-HEMT approach, exploiting the high-voltage capability of silicon Si-IGBTs together with the low switching losses of GaN devices. One of the simplest and cheapest AHMLI configurations is based on a main three-level T-Type SI-IGBTs inverter, that operates at the full *800V* dc input and at very low switching frequency

(<*100Hz*), thus achieving minimal switching losses, and on a GaN-based auxiliary two-level inverter, supplied by a floating dc bus, operates at a much higher switching frequency (around *20kHz*) and requires no external power supply. This arrangement, the main inverter efficiently transfers the entire energy to the motor, while the auxiliary inverter shapes the motor phase current. The T-type topology was selected as it increases the average efficiency [19-20] and eliminates the need for clamping diodes [21-22]. The outcome is a PWM inverter with the voltage-blocking capability of a Si-IGBT inverter and the low switching losses typical of GaN HEMT technology.

The AHMLI therefore achieves higher efficiency than a pure Si-IGBT PWM inverter or a GaN-based 2LI when these operate individually at the same switching frequency. In practice, it delivers efficiency comparable to that of a three-level T-type Si-IGBT inverter operated with step modulation, but with substantially improved voltage and current THD.

5.2 PROPOSED SYSTEM.

A conventional three-phase Si-IGBT-based two-level inverter (2LI) driven by a *10kHz* conventional sinusoidal PWM (SPWM) technique is first considered, as illustrated in Fig. 5.2.

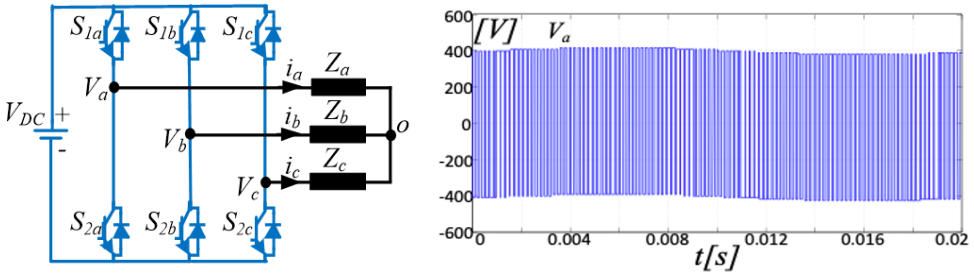


Fig. 5.2 2LI Inverter and output voltage.

The modulation index m is defined as $m_{TLI} = 2\frac{V_m}{V_{DC}}$ where V_m is the amplitude of the sinusoidal voltage reference.

A three-phase three-level T-type inverter (3LI), comprising 12 power devices, driven by a dual-carrier-based three-level sinusoidal PWM (SPWM) technique is taken into account, as shown in Fig. 5.4. This topology is characterized by

three bidirectional switches, which are employed to generate the zero-voltage level.

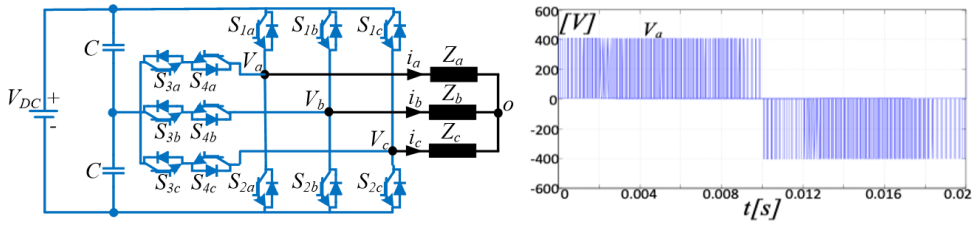


Fig. 5.3 T-Type Inverter and output voltage.

A schematic of the control system managing the PMSM drive is shown in Fig. 5.4. It consists of an inner synchronous current controller, a vector torque controller, and an outer speed control loop and it can be used for both converters.

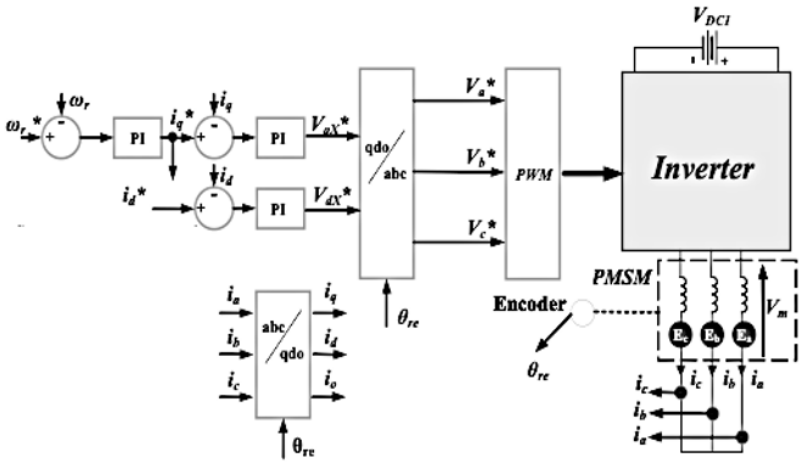


Fig. 5.4 Block diagram of the control system.

According to the AHMLI open-end winding approach, a main MLI, in this case a three-level T-type inverter, delivers the full power to the load, while a smaller auxiliary 2LI acts as an active filter, as shown in Fig. 5.5. Since the auxiliary inverter theoretically provides zero average power, it can be supplied by a floating capacitor, thus avoiding the need for an additional independent power source and preventing the occurrence of zero-sequence currents when a common dc bus is used. Moreover, the dc-link voltage of the auxiliary inverter

is decoupled from the input dc voltage, allowing it to be suitably reduced to achieve an optimal tradeoff between 2LI switching power losses and stator voltage THD. A step modulation technique is adopted for the main MLI to minimize switching losses, while the 2LI employs high-frequency PWM to accurately shape the output voltage.

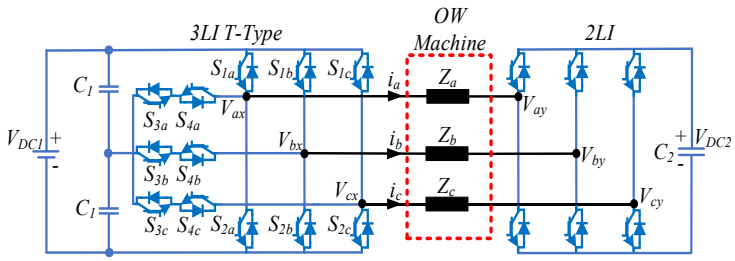


Fig. 5.5 AHMLI Inverter.

5.3 HYBRID SI-IGBT – GAN HEMT AHMLI.

According to the proposed Mixed Si-GaN inverter approach the Si-IGBTs of the auxiliary 2LI are replaced by GaN HEMTs, as shown in Fig. 5.6.

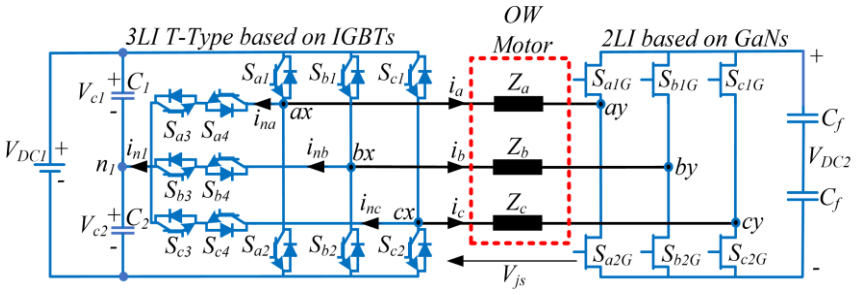


Fig. 5.6 Proposed Mixed Si-GaN inverter.

The 3LI comprises six power switches (S_{j1}, S_{j2}), three bidirectional switches (S_{j3}, S_{j4}) for each phase (j = *a, b, c*), and two DC-link capacitors (C_1, C_2). It delivers the full power to the open-winding motor and operates with step modulation (SM) at the fundamental frequency to minimize switching losses. As a result, the bidirectional switches are not used for current shaping, allowing the use of slower but robust Si-IGBTs. The 2LI, composed of six GaN-based power switches (S_{j1G}, S_{j2G}) and a floating capacitor (C_f), performs three key functions: shaping sinusoidal motor currents, balancing DC-link capacitor voltages, and

controlling the capacitor voltage V_{DC2}. These are achieved using high-frequency sinusoidal PWM (≥*50kHz*), leveraging GaN's fast-switching capability for improved dynamic performance and reduced passive component size, which contributes to overall system compactness and lower weight.

5.3.1 3LI modulation strategy.

The task of the 3LI is to supply the entire power to the motor by operating at the motor's rotor speed frequency *f*, while the switching frequency of the converter is f_{sw}. Assuming a constant DC-Bus voltage V_{DC1} evenly distributed between the two capacitors C_1 and C_2, the voltage V_{jx} between the *jx*-pole terminal *jx* and the DC-Bus midpoint n_1 may take three possible voltage levels, namely $-V_{DC1}/2$, $V_{DC1}/2$, and *0*:

$$V_{jx} = \frac{l_h^{'} - 1}{2} V_{DC1} \quad l_h^{'} = 0, 1, 2 \tag{20}$$

At steady state, the waveform of the output voltage V_{jx} exhibits a three-level stepwise pattern, as illustrated in Fig. 5.7, where θ_{se} is the angular phase of the motor stator voltage V_{js}. According to the Fourier series, the voltage $V_{jx}(\theta_{se})$ can be expressed as the sum of its n-th order harmonic components [23]:

$$V_{jx}(\theta_{se}) = \sum_{n=1}^{+\infty} |V_{jxn}| \sin[n(\theta_{se} - m\pi)] \begin{cases} j = a \;\; m = 0 \\ j = b \;\; m = 1 \\ j = c \;\; m = -1 \end{cases} \tag{21}$$

where $|V_{jxn}|$ is the amplitude of the *n*-th harmonic component and is given by:

$$|V_{jxn}| = \frac{2V_{DC1}}{n\pi} \cos(n\alpha) \tag{22}$$

The amplitude of fundamental component (*n=1*) of V_{jx} is therefore equal to:

$$|V_{jx1}| = \frac{2V_{DC1}}{\pi} \cos(\alpha) \tag{23}$$

From this expression, the switching angle α can be derived as a function of the reference fundamental component $|V_{jx1}^{*}|$:

$$\alpha = cos^{-1}\left(\frac{\pi|V_{jx1}^{*}|}{2V_{DC1}}\right) m_x = \frac{\pi|V_{jx1}^{*}|}{2V_{DC1}} \tag{24}$$

where m_x is the modulation index of the 3LI.

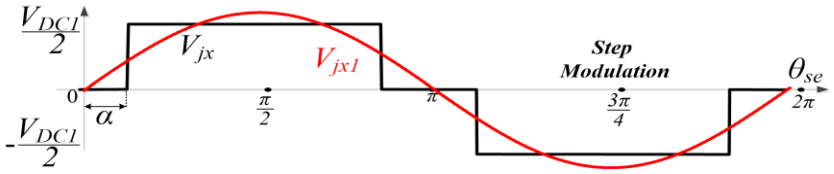


Fig. 5.7 3LI output voltage waveform V_{jx} and fundamental component V_{jx1}.

5.3.2 Mathematical model of the PM synchronous motor.

The proposed Mixed Si-GaN inverter can drive a synchronous or asynchronous OEW machine. In this work, a control algorithm has been implemented to drive a Interior Permanent Magnet Synchronous Motor (IPMSM). The IPMSM mathematical model in a rotating *dq* reference frame with the *d*-axis placed on the direction of minimum magnetic reluctance is given by:

$$\begin{bmatrix} V_{ds}^r \\ V_{qs}^r \end{bmatrix} = \begin{bmatrix} R_s + pL_d & -\omega_{re}L_q \\ \omega_{re}L_d & R_s + pL_q \end{bmatrix} \begin{bmatrix} i_d^r \\ i_q^r \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_{re}\lambda_{pm} \end{bmatrix} \tag{25}$$

$$T_e = \frac{3}{2} PP\left[\lambda_{pm} i_{qs} + \left(L_d - L_q\right) i_{qs} i_{ds}\right] \tag{26}$$

where V^r_{dqs} are the stator *dq*-axes voltages in the rotor reference frame, i^r_{dq} are the stator *dq*-axes currents in the rotor reference frame, L_d and L_q are *d* and *q* axes stator inductances, R_s is the stator resistance, ω_{re} is the angular rotor speed in electrical *rad/s*, λ_{pm} is the permanent-magnet flux linkage, *PP* are the pole pairs, *p* is the derivative operator and T_e is the electromagnetic torque. According to the OEWM configuration, the *dq*-components of stator voltage V^r_{ds} and V^r_{qs} can be written as the difference of 3LI output voltages V^r_{dqx} and the 2LI output voltage V^r_{dqy}. The terms V^r_{dqx} and V^r_{dqy} are the *dq*-axes components of V_{jx} and V_{jy}. Hence, (25) can be written as:

$$\begin{bmatrix} V_{ds}^r \\ V_{qs}^r \end{bmatrix} = \begin{bmatrix} V_{dx}^r - V_{dy}^r \\ V_{qx}^r - V_{qy}^r \end{bmatrix} \tag{27}$$

The matrix transformations are provided in the appendix. The 3LI must synthesize the back-EMF components e^r_{dqs}, which are the largest voltage terms and depend on the angular rotor speed:

$$\begin{bmatrix} V_{dx}^r \\ V_{qx}^r \end{bmatrix} = \begin{bmatrix} e_{ds}^r \\ e_{qs}^r \end{bmatrix} = \begin{bmatrix} pL_d & -\omega_{re}L_q \\ \omega_{re}L_d & pL_q \end{bmatrix} \begin{bmatrix} i_d^r \\ i_q^r \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_{re}\lambda_{pm} \end{bmatrix} \tag{28}$$

while the rest of the voltage term in (25) is generated by 2LI, which is tasked to control the *dq*-axes currents, as explained in the following. Hence, the switching angle *α* is obtained by the back-emf voltage terms:

$$\alpha = cos^{-1}\left(\frac{\pi\sqrt{e_{ds}^{r} + e_{qs}^{r}}}{4V_{DC1}}\right) = cos^{-1}\left(\frac{\pi|e|}{4V_{DC1}}\right) \qquad (\mathbf{29})$$

being $|e| = |V_{jx1}^{*}| = \sqrt{e_{ds}^{r} + e_{qs}^{r}}$.

Table 5.1 3LI switching rules.

3LI J-POLE		
$(2m\pi)/3<\theta_{se}<\alpha+(2m\pi)/3$ $(2m\pi)/3+\pi\ \alpha<\theta_{se}<\pi+\alpha+(2m\pi)/3$ $(2m\pi)/3+2\pi-\alpha<\theta_{se}<2\pi+(2m\pi)/3$	$i_j>0$	**I_a'=1** (S_{j1} ON – S_{j2} OFF) (S_{j3} OFF- S_{j4} ON)
	$i_j<0$	**I_a'=2** (S_{j1} OFF – S_{j2} ON) (S_{j3} ON- S_{j4} OFF)
$(2m\pi)/3+\alpha<\theta_{se}<\pi-\alpha+(2m\pi)/3$ $(2m\pi)/3+\pi+\alpha<\theta_{se}<2\pi-\alpha+(2m\pi)/3$		**I_a'=0** (S_{j1} OFF – S_{j2} OFF) (S_{j3} ON- S_{j4} ON)
j=a→m=0 j=b→ m=1 j=c→ m=2		

The 3LI switching roles are shown in Table 5.1, utilizing the stator voltage phase angle θ_{se} computed from the rotor position θ_r and reference back-emf. The IPMSM is driven through a conventional Vector Control (VC) approach.

5.3.3 2LI Modulation strategy.

The tasks assigned to the 2LI are those to control the electromagnetic torque of the IPMSM, equalize the DC-link capacitors of the 3LI, shape sinusoidally the phase currents, and regulate the floating the 2LI DC-link voltage V_{DC2}. To achieve this with high dynamic performance, the 2LI uses a conventional sinusoidal PWM (SPWM) technique, providing a phase voltage V_{jy}. At the same time, the 3LI provides the back-EMF components as (28) and (29). The voltage V_{jy} switches between two levels, namely $-V_{DC2}/2$ and $V_{DC2}/2$:

$$V_{jy} = \frac{2l_h^{"} - 1}{2} V_{DC2} \qquad l_h^{"} = 0,1 \qquad (\mathbf{30})$$

The phase voltage V_{js} across the *j*-phase winding of the motor is expressed as:

$$V_{js} = V_{jx} - V_{jy} - V_{n1n2} \qquad (\mathbf{31})$$

being V_{n1n2} the Differential-Mode-Voltage (DMV) for an OEWM structure [24].

Due to the 2LI flying DC-Bus, V_{js} depends on the voltage V_{n1n2}, which is expressed as:

$$V_{n1n2} = \frac{1}{3}\left[(V_{ax}+V_{bx}+V_{cx}) - (V_{ay}+V_{by}+V_{cy})\right] \quad (32)$$

The 2LI phase voltage reference V_{jy}^{*} is given by three terms:

$$V_{jy}^{*} = V_{jyCurr}+V_{jyFl}+V_{jyh} \quad (33)$$

where, V_{jyCurr} represents a term related to closed-loop regulation of the phase current and 3LI DC-link voltage equalization, V_{jyFl} is associated with the control of the 2LI floating DC-Bus voltage V_{DC2}, and V_{jyh} is given by predictive shaping of the phase currents. The following sections examine the different terms.

5.3.4 Shaping of phase currents.

According to (20), (30) and (31), the number of potential levels N_{xy} of the voltage $V_{jxy}=V_{jx}-V_{jy}$ is a function of the ratio k_v between the voltages of the two DC-Buses ($k_v=V_{DC2}/V_{DC1}$). According to (32), also the number of potential levels N_{DMV} of the voltage V_{n1n2} is a function of k_v. As a result, the motor phase voltage V_{js} features N_L potential levels, as shown in Table 5.2.

Table 5.2 Voltage Levels v.s. K_v

k_v	1	$0.5<k_v<1$	0.5	$0.25<k_v<0.5$	0.25	$k_v<0.25$
N_{xy}	5	6	4	6	6	6
N_{DMV}	9	13	7	13	9	13
N_L	15	25	11	31	17	31

According to Table 5.2, the voltage ratio k_v is of paramount importance for the proposed system because it affects some important features, such as voltage and current THD_v, THD_i and voltage ratings of 2LI devices. In general, the higher k_v, the higher the voltage stress experienced by power devices of the 2LI and the switching losses, while too low a value of k_v leads to a degradation of the motor phase current waveform. The quantity k_v is linked to the voltage references V_{jy}^{*}, and therefore is a function of all three voltage terms in (33). Simulation tests on Matlab/Simulink have been conducted to evaluate each voltage term of (33). The voltage term V_{jyh} is derived from all the harmonics which must be cancelled. It is given by:

$$V_{jyh}^{*} = \sum_{n=Nmin}^{Nmax} |V_{jxn}| sin[n(\theta_{se} - m\pi)] \begin{cases} j = a \;\; m = 0 \\ j = b \;\; m = 1 \\ j = c \;\; m = -1 \end{cases} \quad (\mathbf{34})$$

where N_{min} and N_{max} are respectively the lowest and highest order of the voltage harmonics generated by the 3LI that the 2LI is tasked to compensate and $|V_{jxn}|$ is given by (26). The voltage ratio k_v is function of m_x, because, according to (34), V_{jyh} depends on the magnitude of the harmonics generated by the 3LI which the 2LI is tasked to compensate. Figure 5.8 illustrates the relationship between the voltage ratio k_v and the THD_v of the motor phase voltage V_{js}, plotted as a function of α and N_{max}, with $N_{min}=5$ and $f_{sw}=50kHz$. Being an isolated OEWM system, ZSC does not circulate; therefore, it is not necessary to eliminate the Zero Sequence Voltage components of (32). This results in a reduction of the required V_{DC2} and, consequently, a reduction of k_v. As N_{max} increases, the required 2LI DC-Bus value V_{DC2} also rises, while the THD_v decreases. Notably, in cases where $N_{max}=13$ and $N_{max}=\infty$, there is a marginal difference in THD_v despite a significant variance in voltage ratio k_v. This observation allows to use a k_v value of *0.25* rather than *0.5*, consequently reducing both the voltage rating of 2LI power switches and power losses. Furthermore, V_{as} can exhibit up to seventeen levels due to the 2LI floating DC-Bus, leading to fluctuations in V_{n1n2}, as described in fig. 5.9. The simulation was conducted with $V_{DC1}=800V$, a voltage gain of k_v equal to *0.25* ($V_{DC2}=250V$), a *50Hz* fundamental frequency *f*, and a *1kHz* 2LI switching frequency. All variables are expressed in per unit (p.u.) with respect to V_{DC1}. The choice of a 2LI switching frequency f_{sw} of *50kHz* is supported in Table 5.3. The THD_v has been evaluated for $k_v=0.25$, six different switching frequencies, and at two different rotor speeds. The results indicate that the minimum value of THD_v is achieved at approximately *50kHz*, and any further increase in switching frequency would only lead to higher power losses without improving THD_v.

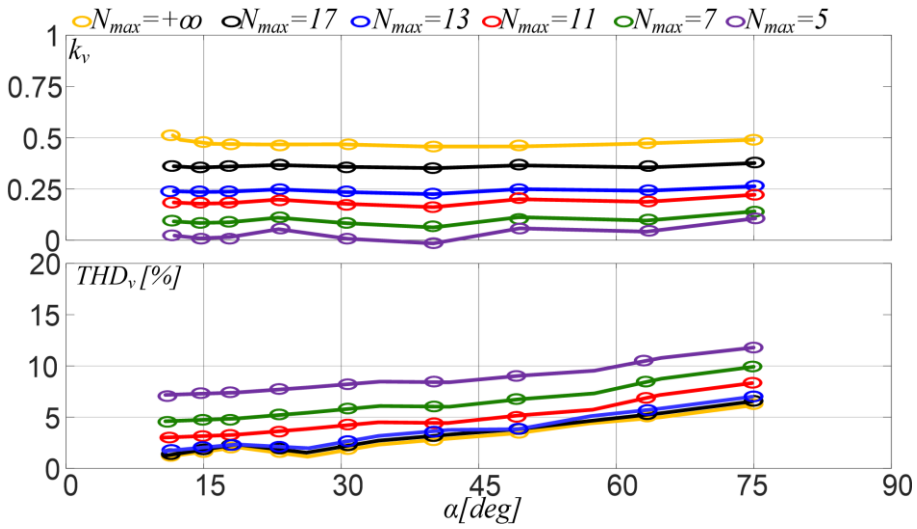


Fig. 5.8 (up) K_v vs. m_x and N_{max}. (down) THD_v vs. m_x and N_{max}.

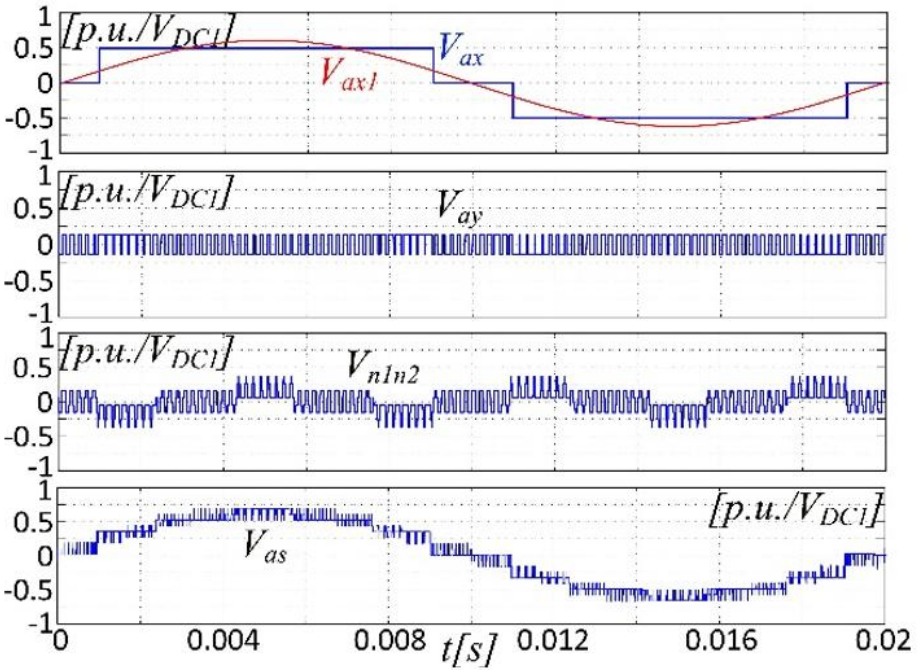


Fig. 5.9 From top: a-phase 3LI output voltage V_{ax}, a-phase 2LI output voltage V_{ay}, voltage V_{n1n2}, a-phase phase motor voltage V_{as} in p.u. with V_{DC1}=800V, k_v=0.25, f=50Hz, f_{sw}=1kHz.

Table 5.3 Voltage THD_v v.s. 2LI switching frequency f_{sw} at k_v=0.25

	2LI Switching frequency						
	500Hz mf=10	**10kHz mf=200**	**30kHz mf=600**	**40kHz mf=800**	**50kHz mf=1000**	**60kHz mf=1200**	**100kHz mf=2000**
THD_v $\omega_r=\omega_b$	43%	8.5%	6.5%	5.7%	4.6%	4.56%	4.54%
THD_v $\omega_r=2\omega_b$	44%	9.5%	7.3%	6.8%	5.5%	5.43%	5.41%

5.3.5 3LI DC-Link voltage equalization and torque control.

The term V_{jyCurr} in (33) represents the voltage component used for closed-loop regulation of the phase current i_j and 3LI DC-link voltage equalization. As mentioned earlier, a vector control strategy is employed, based on Maximum Torque per Ampere (MTPA) and Field Weakening (FW) methods [25]. The output of the speed regulator provides the q-axis component of the stator current, i_{qm}, while the d-axis component, $i_{d,}$ is obtained from the MTPA trajectory. The q-axis reference component of the phase current is given by the sum of i_{qm} and a term i_{qn}, which is used to balance the voltages across the capacitors of the 3LI:

$$i_q^* = i_{qm}^* + i_{qn}^* \tag{35}$$

Equalization of the voltages of the capacitors in the 3LI DC-link is achieved leveraging the connection which periodically occurs among the motor, 2LI, and DC-bus midpoint n_1. This strategy allows dynamic equalization of the voltages across the two DC-link capacitors, denoted as V_{C1} and V_{C2}. Each phase leg j=*a,b,c* of a 3LI inverter can be switched into one of three possible states:

- P (positive): Switches S_{j1} and S_{j3} are turned on, yielding an output voltage of $+V_{DC1}/2$;
- N (negative): Switches S_{j2} and S_{j4} are turned on, yielding an output voltage of $-V_{DC1}/2$;
- O (zero): Switches S_{j3} and S_{j4} are turned on, leading to 0 V output.

As shown in the vector diagram in Fig. 5.10, a 3LI inverter allows for *27* switching combinations across three phases, three of which are zero vectors, and *24* are active. Unlike conventional methods like sinusoidal PWM or SVM, step modulation produces a distinct switching pattern. The set of active states

varies with the modulation index m_x, defined by (24) as a function of the switching angle α. Based on α, three operating ranges can be identified:

- High modulation index: $0<\alpha<30°$;
- Medium modulation index: $30°<\alpha<60°$;
- Low modulation index: $60°<\alpha<90°$.

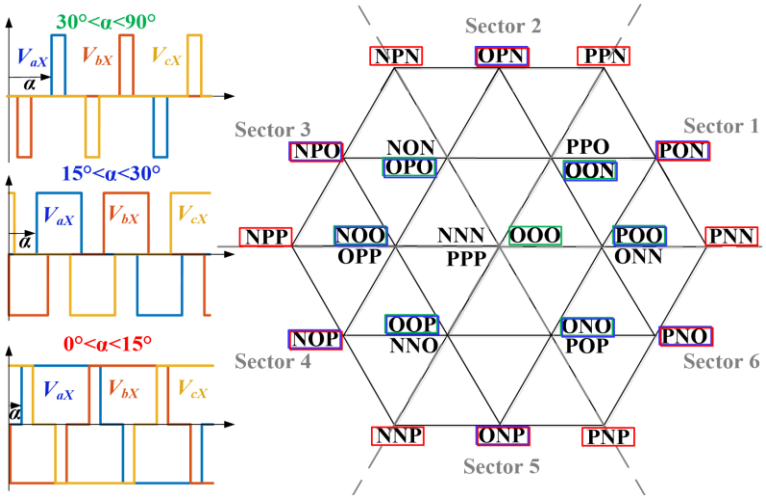


Fig. 5.10 Voltage vector diagram of the 3LI.

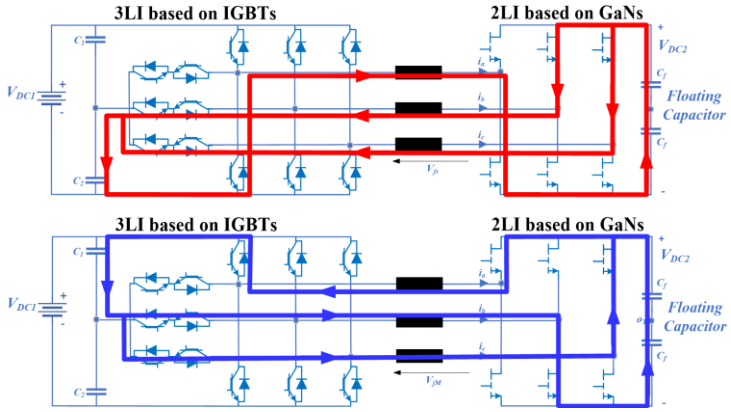


Fig. 5.11 Voltage equalization for low and medium m_x (NOO): $V_{C1}>V_{C2}$ (top) and $V_{C1}<V_{C2}$ (down).

Each range results in a distinct switching pattern and a different subset of states being used, as shown in Fig. 5.10. For effective control of the capacitor voltages, it is essential to act during those switching states where only one capacitor is

directly connected to the 2LI through a motor phase. For example, in the NOO state (which can appear in both low and medium modulation index ranges), capacitor C_2 is directly connected to the 2LI, Fig. 5.11. If $V_{C2}<V_{DC1}/2$, the 2LI can charge C_2, helping to restore voltage balance when $V_{C1}>V_{C2.}$ To discharge C_2, energy can be diverted to charge C_1, which is possible during the POO state, also available in both low and medium modulation index ranges.

Table 5.4 3LI DC-Bus voltages equalization rules.

i_{qn}^* is added to i_{qm}^* **if OON,OPO,NOO, OOP,ONO,POO**	$V_{C1}>V_{C2}$ **and**	$i_{ag}<0$ **and** (S_{b1G} ON or S_{c1G} ON) **or** $i_{bg}<0$ **and** (S_{a1G} ON or S_{c1G} ON) **or** $i_{cg}<0$ **and** (S_{a1G} ON or S_{b1G} ON)
	$V_{C1}<V_{C2}$ **and**	$i_{ag}>0$ **and** (S_{b2G} ON or S_{c2G} ON) **or** $i_{bg}>0$ **and** (S_{a2G} ON or S_{c2G} ON) **or** $i_{cg}>0$ **and** (S_{a2G} ON or S_{b2G} ON)

In contrast, under high modulation index conditions, large vector states such as PNN**,** PPN**,** NPN**,** NPP**,** NNP**,** and PNP result in both capacitors being connected in series across the full DC voltage V_{DC1}. This configuration naturally balances the capacitor voltages toward $V_{DC1}/2$*,* assuming ideal conditions. To actively regulate the capacitor voltages, positive or negative active power exchange is necessary. This is achieved by superimposing a current component along the *q*-axis i_{qn} onto the stator motor current i_{qm}, (35). The magnitude and direction of i_{qn} are determined by the desired capacitor voltage balance V_{C1}-V_{C2}=*0*, and by referencing Table 5.4, which maps the switching states to capacitor connectivity via the 2LI.

5.3.6 2LI DC-Link regulation.

The floating capacitor C_f of the 2LI is charged whenever the active power P_y is positive. Conversely, a negative P_y causes the capacitor C_f to discharge.

According to a dq reference system, the active power P_y absorbed by the 2LI is:

$$P_y = \frac{3}{2}\left(V_{qFl} i_q + V_{dFl} i_d\right) \quad (\mathbf{36})$$

The reactive power Q_y is in practice forced to zero to minimize the power losses and the DC bus voltage, hence the reference voltages V_{qFl} and V_{dFl} are given by:

$$V_{dFl} = 0 \quad (\mathbf{37})$$

$$V_{qFl} = \frac{2}{3}\frac{P_y}{i_q} \quad (\mathbf{38})$$

where P_y represents the output of the PI regulator tasked to control V_{DC2}.

5.4 CONTROL SYSTEM.

The control scheme, illustrated in Fig. 5.12, is based on a VC strategy that integrates the MTPA and FW methods. It is structured around five main components: predictive terms calculated using (28) for the 3LI, a floating capacitor voltage control for V_{DC2}, a balancing control for the 3LI capacitors, a *qd* current controller, and harmonic compensation. The inputs of MTPA and FW blocks are the rotor angular speed ω_r, the torque reference T_e^* and the inverter rated voltage V_{max}. The predictive block outputs the *qd*-axis back-EMF components, calculated using (25), from which the switching angle α and the phase angle θ_{se} are derived for implementing the step modulation. The V_{DC2} control block outputs the *q*-axis voltage component V_{qFl}^*, while $V_{dFl}^*$is set to zero, as in (37) and (38). The inverse Park transformation then provides the voltage references V_{jyFl}^*. The capacitor voltage balancing block for V_{C1} and V_{C2} generates the quantity i_{qn}, which is added to the stator current component i_{qm} from the current control loop, as in (35). The outputs of the *qd* current controller are V_{qCurr}^* and V_{dCurr}^*, which are then transformed into V_{jyCurr}^* through the inverse Park transformation. The final harmonic compensation block generates the term V_{jyh}^*, as defined in (33). The sum of all three terms provides the voltage reference for the 2LI V_{jy}^*, as expressed in (34).

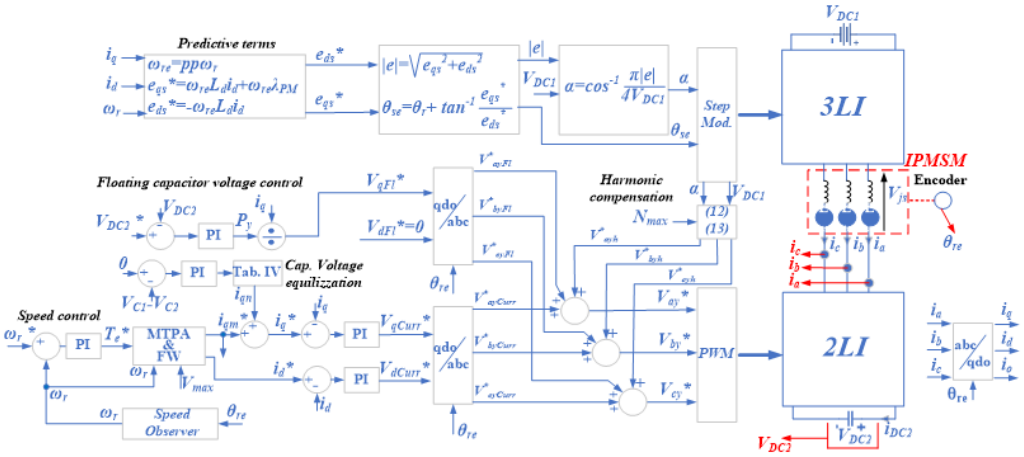


Fig. 5.12 Control system of IPMSM.

5.4.1 DC Link capacitors sizing.

In this section, the capacities C_1 and C_2 of the 3LI and the floating capacitor C_f of 2LI have been sized by imposing maximum voltage ripple $\Delta V_C=5\%V_{DC1}$ and a maximum total voltage harmonic distortion ($THD_{Vmax}=10\%$) as requirements. The most critical sizing concerns the capacitors C_1 and C_2, as the 3LI operates at low switching frequency f. The maximum voltage ripple on C_1 e C_2 naturally depends on the switching states and therefore on the modulation range. Under the hypothesis that $C_1=C_2=C$, it can be found that neutral point voltage V_{n1}:

$$\frac{dV_{n1}}{dt}=\frac{d(V_{c1}-V_{c2})}{dt}=\frac{1}{C}i_{n1}=\frac{1}{C}\sum_{j=a,b,c}i_{n1} \qquad (39)$$

where i_{nj} is the contribution of the j leg to the current i_{n1}, being:

$$i_{n1}=i_j s_j \qquad (40)$$

where $i_j=I\times sin(\omega_{se}t+\varphi)$ is the phase current, ω_{se} is the angular stator voltage speed while s_j ($0<s_j<1$) is defined as:

$$s_j=\frac{T_{Oj}}{T} \qquad (41)$$

where T is the inverse of the switching frequency f of 3LI and T_{Oj} the amount of time within T for which the j leg takes the switching combination O. The quantity s_j can be written as:

$$s_j = 1 - m_x \, |sin(\omega_{se} t)| \tag{42}$$

Hence, the contribution of the *j* leg to the current i_{n1} is:

$$i_{n1j} = I \times sin(\omega_{re} t + \varphi) \times [1 - m_x \, |sin(\omega_{se} t)|] \tag{43}$$

while the neutral current i_{n1} is given by:

$$i_{n1} = i_{n1a} + i_{n1b} + i_{n1c} \; = \; 0.5 \times I \times m_x \times sin(3\omega_{se} t + 3\varphi) \tag{44}$$

Under steady-state conditions, the current i_{n1j} oscillates at the fundamental frequency *f,* with amplitude depending on the phase current, the voltage-current phase angle φ, and the modulation index. This induces a third-harmonic oscillation in i_{n1}, shaped by the phase angle φ. Substituting (39) into (40), the neutral point voltage V_{n1} becomes::

$$\begin{cases} V_{n1} = \dfrac{1}{C} \int i_{n1} \, dt = -\dfrac{m_x \times I}{6 \times \omega_{se} \times C} cos(3\omega t + 3\varphi) = \Delta V_c \\ V_{c1} = \Delta V_c + 0.5 V_{DC1} \\ V_{c2} = \Delta V_c + 0.5 V_{DC1} \end{cases} \tag{45}$$

where $\omega_{se}=2\pi f$, and *I* the magnitude of motor current. As shown in (45) the capacitor voltage ripple ΔV_C depends on current *I*, angular frequency ω_{se}, and capacitance *C*.

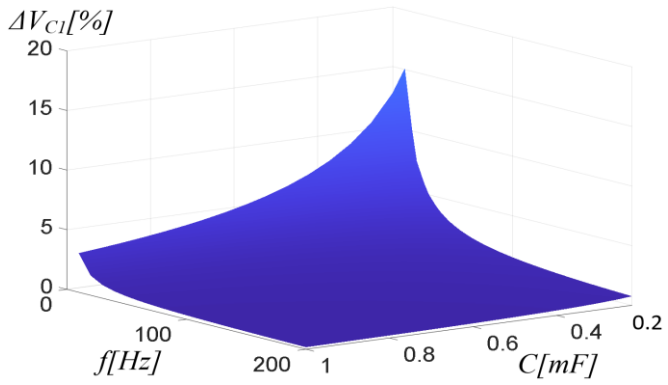


Fig. 5.13 3LI DC-Link capacitor voltage ripple ΔV_C as a function of fundamental frequency f and capacitance C_1 at α=40°, P_n=10kW, V_{DC1}=800V, V_{DC2}=250V, f_{sw}=50kHz.

Figure 5.13 shows ΔV_C versus frequency *f* and *C* at *10kW, 14A*, and worst-case *α= 40°*. To keep ΔV_C<5% of V_{DC1}, at least *0.6mF* is needed. The effect on motor

voltage THD_v is also evaluated for k_v=*0.31.* Figure 5.14 shows the THD_v as a function of capacitance *C* and fundamental frequency *f* under nominal current. Capacitor size significantly affects THD_v, especially at low speed and low capacitance. To maintain THD_v<*10%,* a capacitance of around *800 μF* is required, which also ensures ΔV_C<*5%,* yielding even better performance. For the 2LI capacitor C_f, its current rating I_{cf}, and the voltage ripple ΔV_{cf} in a conventional PWM inverter [32] follow the well-known relation:

$$\begin{cases} \Delta V_{cf} = \dfrac{V_{DC2} \times I}{4 \times f_{sw} \times C_f} = \dfrac{k_v \times V_{DC1} \times I}{8 \times f_{sw} \times C_f} \\ I_{cf} > \dfrac{6 \times I}{5} \end{cases} \quad (46)$$

To achieve a capacitor voltage ripple ΔV_{Cf} lower than *5%*V_{DC2} (*13V* out of *250V* with k_v=*0.31*), a capacitance greater than *700μF* is sufficient. Since at rated conditions the load current is *14A*, a capacitor with a current rating I_{cf} greater than *17A* should be selected. Therefore, based on the analysis of commercially available capacitors, a *820μF* capacitance has been selected for all the capacitors.

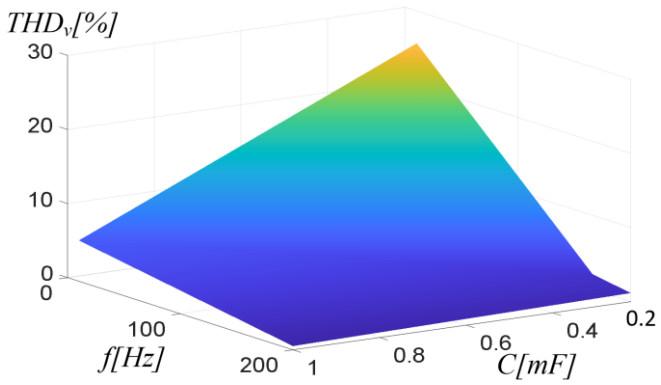


Fig. 5.14 THD_v as a function of frequency f and capacitance C_1 at α=40°, P_n=10kW, V_{DC1}=800V, V_{DC2}=250V, f_{sw}=50kHz.

5.5 SIMULATION RESULTS.

Simulation tests have been conducted on the Matlab/Simulink platform considering a *10kW* IPMSM, whose parameters are listed in Table 5.5. Figure 5.15 illustrates the simulation of the system operating under VC at *1500 rpm*, with f_{sw}=*50kHz*, C_1=C_2= C_f=*1mF*. The control algorithm performs effectively for the 2LI

when the voltage ratio k_v is adjusted at *0.31 (Δk_v=0.06),* enabling the Mixed Si-GaN inverter to operate with six output voltage levels. Predictive phase current shaping eliminates low-frequency harmonics, reducing torque ripple and current THD_v. Using GaN devices switching at *50kHz* under current control*,* compared to the Si-MOSFETs at *10-20kHz* in [14], further lowers voltage THD_v, Table 5.6. Specifically, the values in Table 5.6 were obtained with k_v=*0.31* and current control, whereas those in Table 5.3 were obtained with k_v=*0.25* and without current control. With N_{min}=5 and N_{max}=13, a higher modulation frequency m_f improves the synthesis and suppression of higher-order harmonics, especially at high speeds. At $\omega_r=\omega_b$, the fundamental frequency *f* is *50Hz* (*13th* harmonic is *650Hz*), while at $\omega_r=2\omega_b$, *f=100Hz* (*13th* harmonic is *1300Hz).* A higher m_f enables better harmonic shaping, reducing THD_v and enhancing system smoothness and performance.

Table 5.5 Parameters of the IPMSM.

P_n [kW]	V_s [V]	ω_b [rad/s]	Ld [mH]	Lq [mH]	R_s [Ω]	pp
10	400	1500	0.88	1.62	0.39	2

No significant improvements in THD_v are observed for switching frequencies above *50kHz*, which has therefore been selected in the project. The performance in equalizing the voltages across *C1* and *C2* is assessed in Fig. 5.16, where the motor is spinning at *1500rpm* at 80% of the rated torque with V_{DC1}=*800V,* V_{DC2}=*250V*. A *500Ω* resistor is connected in parallel to *C1* to generate a persistent voltage unbalance. When the voltage equalization is activated, V_{C1} is quickly made equal to V_{C2}.

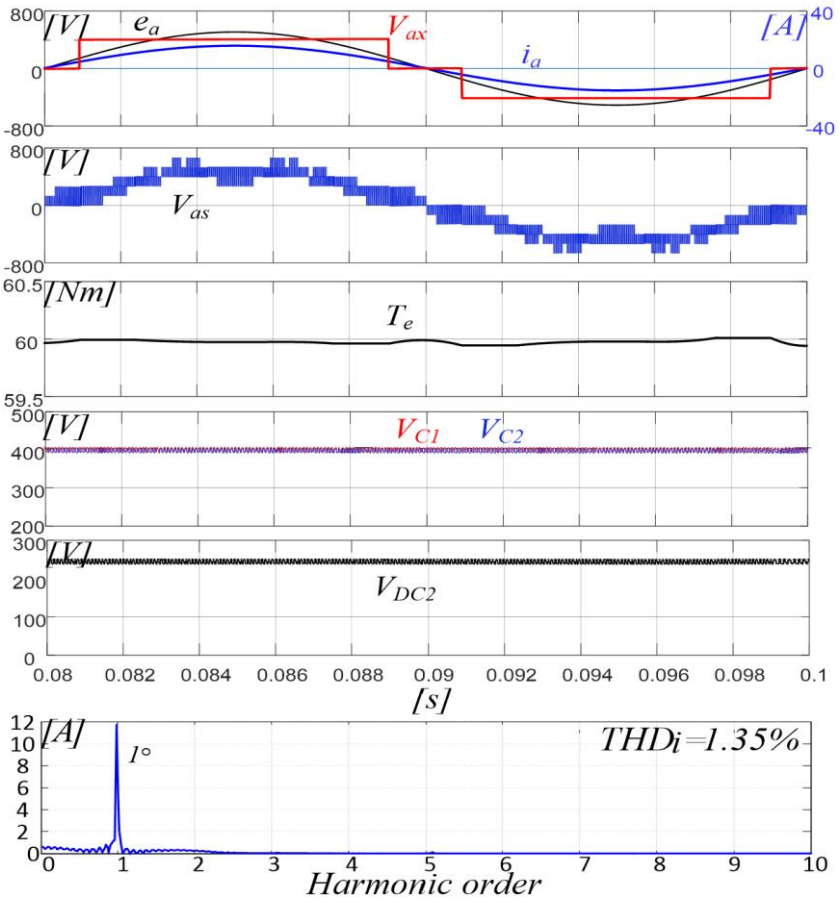


Fig. 5.15 From top to down: V_{ax}, i_a and back EMF e_a, V_{as}, torque T_e, V_{C1}, V_{C2}, V_{DC2}, i_a harmonic spectrum. ω_b=157rad/s, V_{DC1}=800V, V_{DC2}=250V.

Table 5.6 Voltage THD_v v.s. 2LI switching frequency f_{sw} at k_v=0.31 under current control

	2LI Switching frequency						
	500Hz mf=10	**10kHz mf=200**	**30kHz mf=600**	**40kHz mf=800**	**50kHz mf=1000**	**60kHz mf=1200**	**100kHz mf=2000**
THD_v $\omega_r=\omega_b$	42%	8.4%	6.43%	5.71%	4.58%	4.53%	4.52%
THD_v $\omega_r=2\omega_b$	44%	9.53%	7.34%	6.7%	5.3%	5.42%	5.4%

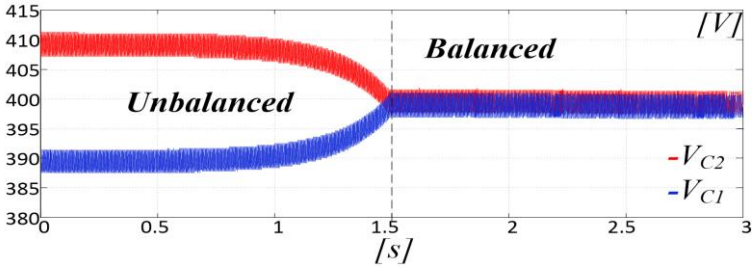


Fig. 5.16 V_{C1} and V_{C2} (α=17°, w_r=1500rpm, V_{DC1}=800V, V_{DC2}=250V, 80% rated current).

5.6 DEVELOPMENT OF MIXED SI-GAN STRUCTURE.

After designing the Mixed Si-GaN inverter with the aid of simulations, a *10kW* prototype was developed using Allegro/OrCAD software. Table 5.7 shows the main project parameters obtained by design. The voltage ratio k_v=*0.31* was selected to meet the design goals for the 2LI. A switching frequency of *50kHz* was chosen to minimize voltage THD_v and reduce capacitor ripple, improving upon the results in [14]. It will be experimentally shown that *50kHz* outperforms *100kHz*, as it achieves the same THD_v but with lower losses.

Table 5.7: Parameters of Mixed Si-GaN.

I_n	ΔV_C	ΔV_{Cf}	$C_1=C_2$	C_f	THD_{Vmax}	k_v	f_{sw}	V_{DC1}	V_{DC2}
14A	<5%	<5%	820μF	820μF	10%	0.31	≥50kHz	800V	250V

The 3LI power stage uses a single three-phase T-Type SIi-IGBT module (NXH40T120L3Q1, *1200V, 40A*), while the 2LI employs GaN Systems GS66516B devices. Each NXH40T120L3Q1 channel contains two *1200V, 40A*

Si-IGBTs with inverse diodes and two *650V, 25A* Si-IGBTs with inverse diodes. A custom motherboard integrates the gate driver circuits for both inverters, as shown in Figure 5.17, with *12* gate drivers (1EDI60N12AF) for the 3LI module, six input channels for the 2LI, and 12 isolated DC-DC converters. The power modules are mounted on the underside of the motherboard for direct contact with the heatsinks. The system is enclosed in an aluminium case, as shown in Fig. 5.18. Additional boards include the 2LI DC-Bus floating capacitor C_f and V_{DC2} voltage sensing, 3LI capacitors C_1 and C_2 with their voltage sensing, motor current sensing, and a DC power supply (*5V, 12V*) for the gate drivers and sensing circuits. Table 5.8 summarizes the prototype's main characteristics.

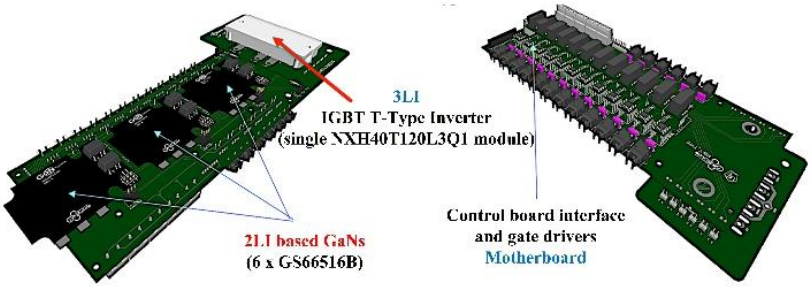


Fig. 5.17 Prototype.

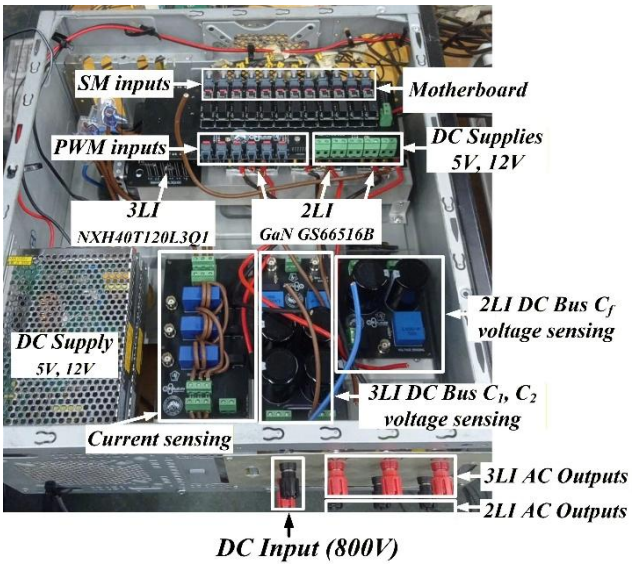


Fig. 5.18 Developed Mixed Si-GaN inverter prototype.

5.7 EXPERIMENTAL TESTS.

The experimental tests were carried out by connecting the *10kW* three-phase IPMSM described in Table 5.5 to the mixed Si-GaN inverter, with an *11kW* induction motor (IM) used as the load and supplied by a second PWM inverter operating under VC. Three differential voltage probes, three Hall-effect current probes, a digital oscilloscope, and a power analyzer were used. Furthermore, a thermal analysis of the GaN modules was conducted during one hour of continuous operation. Indeed, as shown in Fig. 5.19, it can be observed that the modules maintain perfectly acceptable temperatures (around 31°C) even when operating at the 10kW limit of the tested prototype.

Table 5.8 Parameters of Mixed Si-GaN prototype.

Prototype			
Total Weight	10kg	**Volume**	0.02mx0.045mx0.04m
Rated power	10kW	**DC Link Capacitors**	2 x 820µF 500V
Input DC voltage	800 V	**Switching frequency**	f=0-200Hz
Output AC voltage	400V	**Si-IGBTs**	NXH40T120L3Q1 T-Type module: 6x1.2kV, 40A, 6x650V, 25A
Rated power	10kW	**DC Link Capacitors**	820µF 500V
Input DC voltage	<400V	**Switching frequency**	f_{sw}=50kHz
Output AC voltage	200V	**GaNs**	6 GaN GS66516B, 650V, 47A
N_{min}	5	**N_{Max}**	13
Motherboard			
Gate driver	1EDI60N12AFT		
Isolated DC-DC	NMH0515SC, $5V_{in}$, $\pm15V_{out}$		
Optical fiber	HFBR-1521Z		
DC input supplies	5V, 12V		

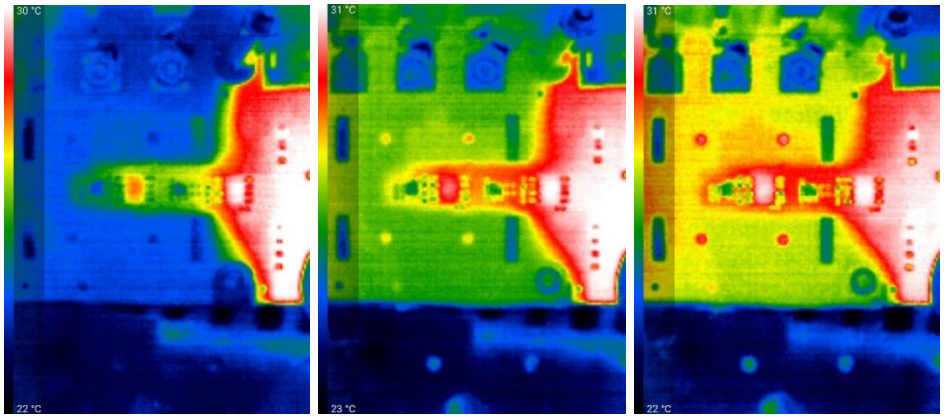


Fig. 5.19 Thermal analysis of GaN modules (one-hour continuous operation): (left) 0% power; (center) 50% power; (right) 100% power.

Not only does the power analyzer measure the power at the DC link of the 3LI and the power at the input of the motor stator, but it also evaluates the total harmonic distortion of the stator voltage and current, the reactive power and power factor. The measured efficiency η refers only to the power converter, being not affected by IPMSM power losses. The control algorithm of Fig. 5.5 was implemented on the DSpace MicroLabBox platform, with gate signals transmitted to the inverter board via an optical fiber transmitter. The IFOC control of the Induction Motor acting as load was implemented on the DSpace 1103 platform. The dead time for the 2LI was set to *300ns*, while the dead time for the 3LI was set to *1µs*. A *5000ppr* encoder provides information on the angular position of the generator shaft.

5.7.1 Steady-state experimental tests.

Several tests were carried out with varying the motor speed and so the fundamental frequencies *f* (*50Hz, 100Hz*, and *200Hz*), varying 2LI capacitor voltage V_{DC2} (*250V, 300V, 350V*, and *400V*), with f_{sw} of the GaN devices at *50kHz*. Figure 5.20 shows the distribution of losses in both the 3LI and 2LI converters as a function of the capacitor voltage V_{DC2}. Losses in the 3LI remain constant, while only the switching losses in the 2LI vary, which is expected. The switching losses in the 3LI are nearly zero due to the low-frequency modulation strategy. The inverter's performance, including efficiency, THD_v, and CMV, depends heavily on the 2LI's V_{DC2} voltage and switching frequency f_{sw}. Several measurements were taken under different conditions. Fig. 5.21 shows the

motor's a-phase voltage V_{as}, the 3LI's a-phase output voltage V_{ax}, the 2LI's a-phase output voltage V_{ay}, and the motor currents i_{abc} under *10kW* load, ω_r*=157rad/s.* Due to a limited number of oscilloscope channels, V_{C1} and V_{C2} are shown in the same figure. Fig. 5.21a-c are for *f=50 Hz*, and fig. 5.21b-d are for *f=200 Hz*, with f_{sw}*=50 kHz* for the 2LI. Fig. 5.22 shows the efficiency of the inverter as a function of V_{DC2} (varied between *250V* and *400V*), load, and f_{sw} at fundamental frequency *f=100Hz* was varied between *250V* and *400V*. The equalization of voltages V_{C1} and V_{C2} is working well, as evidenced by the fact that the V_{ax} voltage is perfectly symmetrical in its positive and negative values.

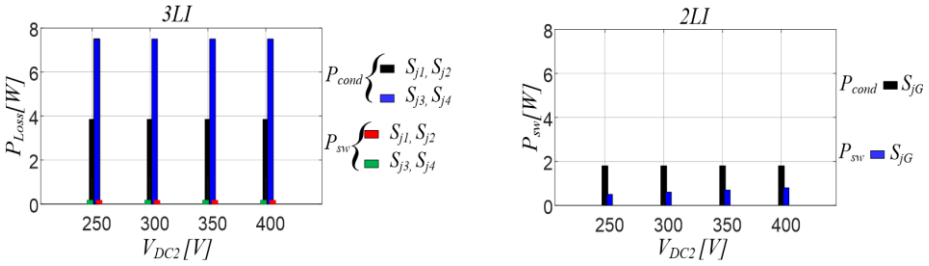
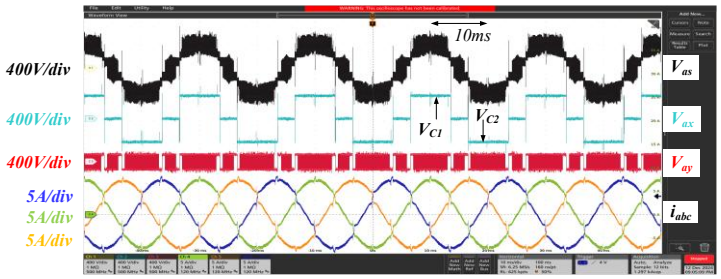
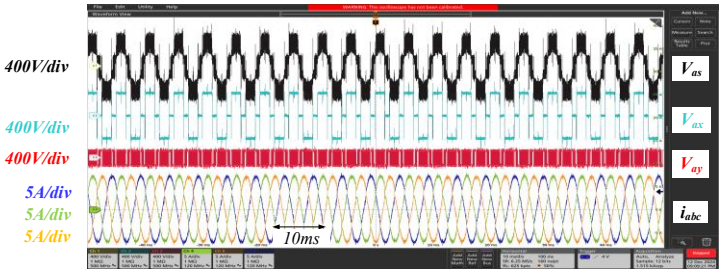


Fig. 5.20 Distribution of power losses versus V_{DC2}. (left) 3LI. (Right) 2LI. P_n=10kW, V_{DC1}=800V, f_{sw}=50kHz.



(a)



(b)

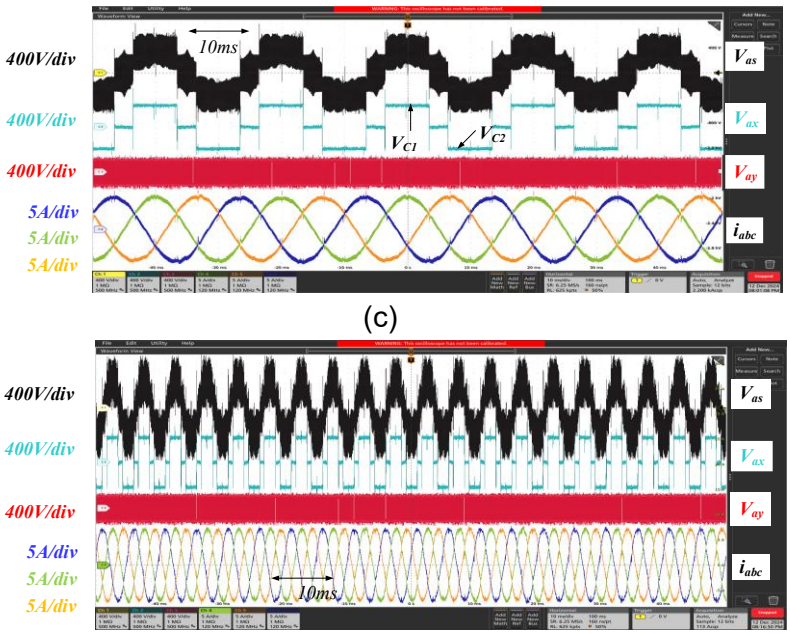


Fig. 5.21 Steady State Tests at 10kW, V_{DC1}=800V, f_{sw}=50kHz. (a,c) f=50Hz. (b,d) f=200Hz. (a,b) V_{DC2}=250V, (c,d) V_{DC2}=400V.

At a fixed switching frequency f_{sw}, maximum efficiency occurs at full load with V_{DC2}=250V (k_v=0.31), as GaN switching losses are linked to drain-source voltage. Although V_{DC2}=250V is optimal for efficiency, it results in higher THD_v, though still within the 10% limit, as shown in Fig. 5.23. Conversely, increasing the switching frequency from *50kHz* to *100kHz* does not improve THD_v but reduces efficiency.

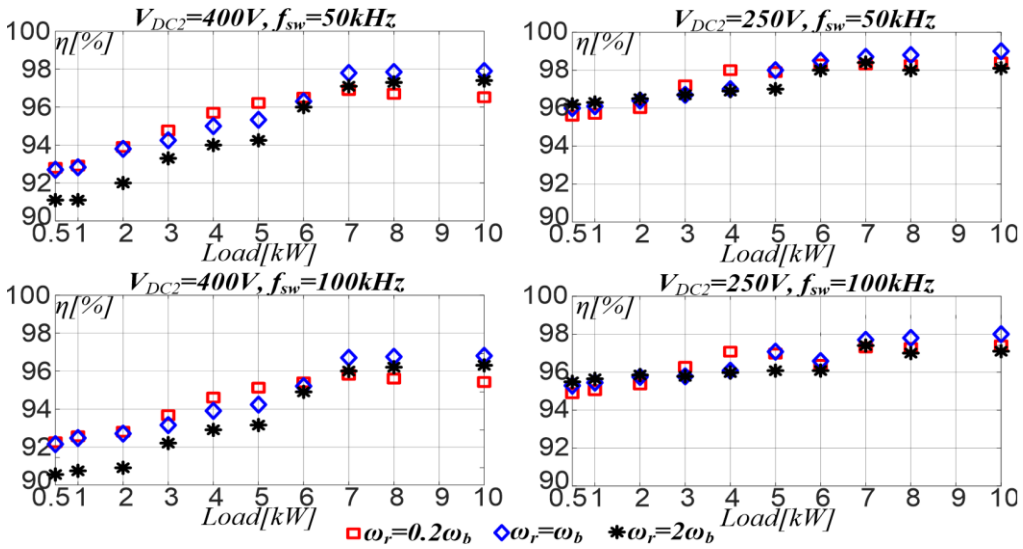


Fig. 5.22 Efficiency versus Load, ω_r, V_{DC2}, and switching frequency f_{sw}.

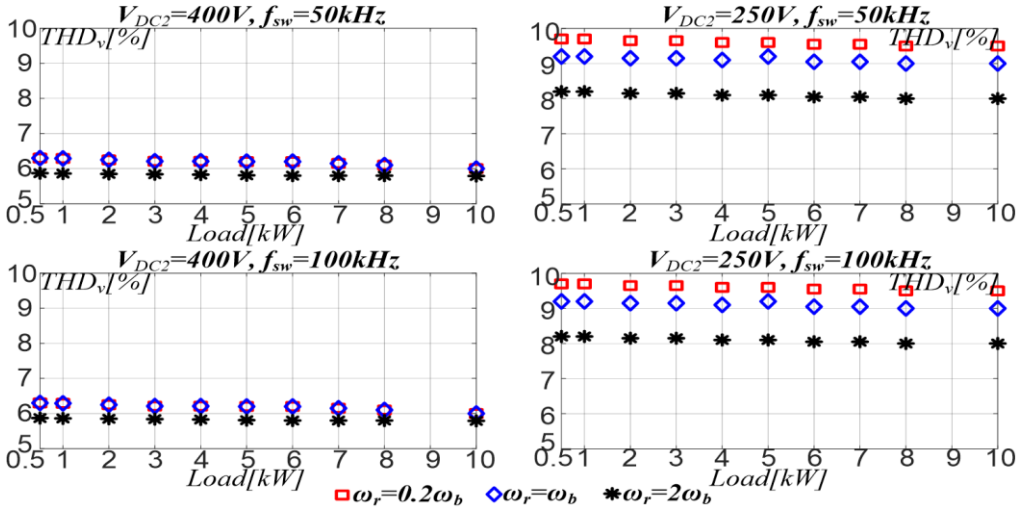


Fig. 5.23 THD_v of V_{as} versus Load, ω_r, V_{DC2}, and switching frequency f_{sw}.

As shown in Fig. 5.24, the CMV varies with V_{DC2}. At V_{DC2}=*250V*, the CMV peak reaches approximately $0.32V_{DC1}$, which is lower than that of a conventional two-level inverter ($0.5V_{DC}$).

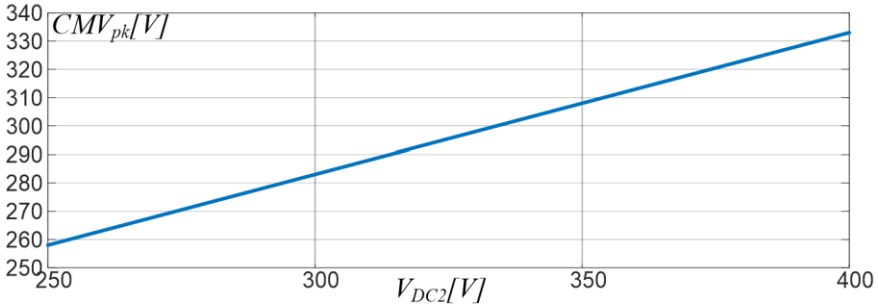


Fig. 5.24 CMV peak value V_{DC2} at f=50Hz, 50kHz and 10kW.

5.7.2 Dynamic tests.

Dynamic tests were conducted, particularly focusing on the control of the V_{DC2} voltage and the current control. A frequency transient from *200Hz* to *50Hz* is shown in Fig. 5.25. Fig. 5.26 (up) shows a variation of the V_{DC2} voltage from *350V* to *250V* with a 2.*5kW* load at *50kHz*, while Fig. 5.26 (down) shows a variation of current from *5A* to 2.*5A*.

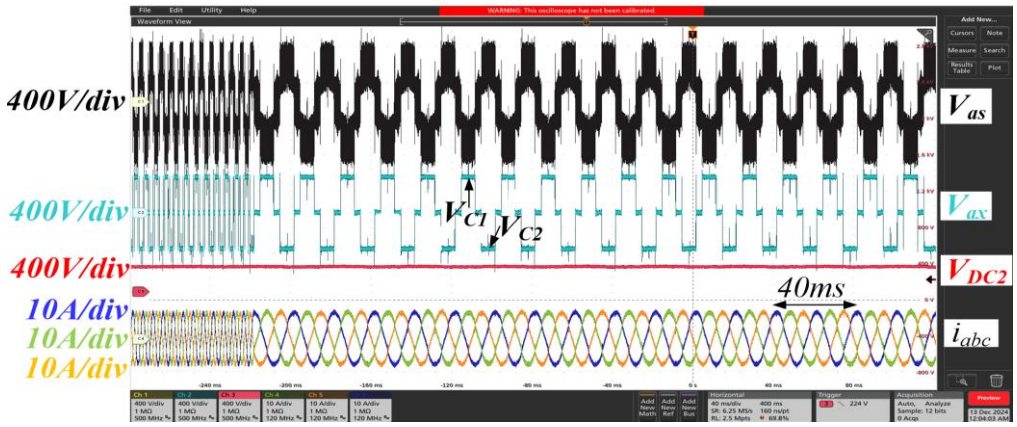


Fig. 5.25 Variation of fundamental frequency f from 200Hz to 50Hz. (5kW, f_{sw}=50kHz, V_{DC2}=250V).

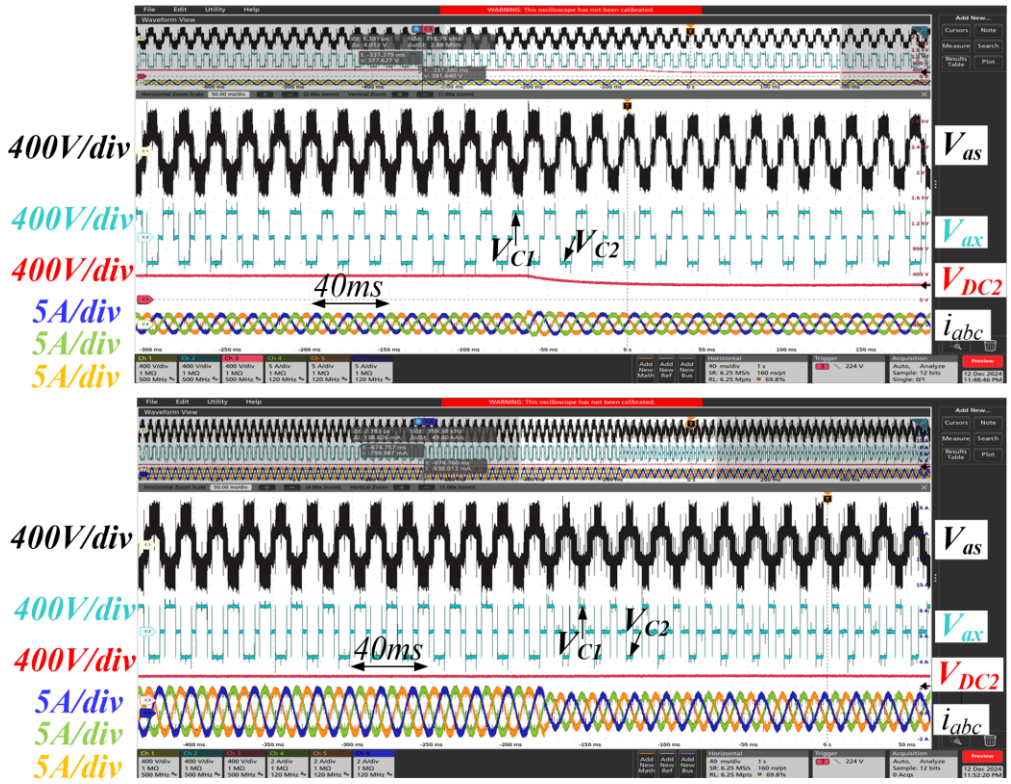


Fig. 5.26 (up) Variation of V_{DC2} from 350V to 250V, 2.5kW; (down) Variation of stator current from 5A to 2.5A. (f_{sw}=50kHz, f=50Hz).

A torque inversion for regenerative braking is described in Fig. 5.27. During the test, the rotor speed was maintained constant at *150rad/s* using the IM. The setup successfully demonstrated bidirectional operation, with the system operating effectively both in motoring mode and in regenerative braking. The motor currents are perfectly sinusoidal, and the V_{ax} voltages are symmetrical, confirming the effective equalization of V_{C1} and V_{C2}. Based on the obtained results, the best choice in terms of THD_v, power losses, and CMV is k_v=*0.31,* V_{DC2}=*250V*, f_{sw}=*50kHz.*

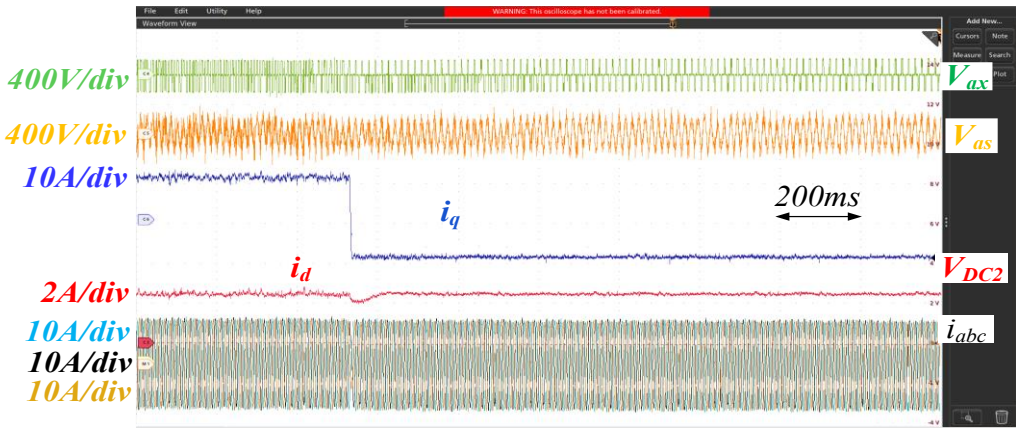


Fig. 5.27 Torque inversion, variation of i_q from 5A to -5A. (f_{sw}=50kHz, f=50Hz, V_{DC2}=250V, i_d=2A, ω_r=150rad/s).

5.8 COMPARISON WITH OTHER TOPOLOGIES.

A comparison in terms of efficiency, power quality, *CMV*, and component cost has been performed considering 9 topologies, as listed in Table 5.9. Topologies A and B correspond to conventional two PWM 2LIs using Si-IGBTs and SiC-MOSFETs, respectively, both driving a star-connected motor. Topologies C and D are three-level NPC inverters, the former based on Si-IGBTs with silicon clamped diodes, and the latter on GaN-HEMTs with SiC clamped diodes. Topologies E, F, and G represent three-level T-Type inverters, implemented with Si-IGBTs, SiC-MOSFETs, and a hybrid SiC/GaN combination, respectively. Topology H considers a symmetrical open-end winding inverter fully based on GaN devices. Finally, topology L is the proposed one, while in Topology I Si-MOSFETs are used instead of GaNs in the 2LI.

Table 5.9 Topologies under comparison.

Top.	Mot. Conn	N_L	INVERTER 1		INVERTER 2	
			Topology/ Modulation	Device	Topology/ Modulation	Device
A	Star	2	2LI / PWM	Si-IGBTs-IKZA40N120CS7	\	\
B	Star	2	2LI / PWM	SiC-IMBG120R034M2HXMA1	\	\
C	Star	3	NPC / PWM	Si-IGBTs-IKW40N65ET7XKSA Si Diode-IDWD40E65E7	\	\
D	Star	3	NPC / PWM	GaN-HEMTs - GS66516B SiC Diode-IDW40G120C5B	\	\
E	Star	3	T-Type / PWM	Si-IGBTs-IKZA40N120CS7, IKW40N65ET7XKSA1	\	\
F	Star	3	T-Type / PWM	SiC-IMBG120R034M2HXT, IMBG65R026M2H	\	\
G	Star	3	T-Type / PWM	SiC-IMBG120R034M2HXTMA1 GaN-HEMTs-GS66516B	\	\
H	OEW	3	2LI / PWM	GaN-HEMTs - GS66516B	2LI / PWM	GaN-HEMTs - GS66516B
I	OEW	6	T-Type / SM	Si-IGBTs-IKZA40N120CS7, IKW40N65ET7XKSA1	2LI / PWM	Si-MOSFETs IPW60R031CFD7XKSA1
L	OEW	6	T-Type / SM	Si-IGBTs-IKZA40N120CS7, IKW40N65ET7XKSA1	2LI / PWM	GaN-HEMTs - GS66516B

Table 5.10 lists device types, and individual cost. Table 5.11 compares all topologies in terms of the number of voltage levels N_L, number of silicon devices $N_{sw\text{-}Si}$, number of SiC devices $N_{sw\text{-}SiC,}$ number of GaN devices $N_{sw\text{-}GaN}$, number of silicon diodes $N_{d\text{-}Si}$, number of SiC diodes $N_{d\text{-}SiC}$, number of capacitors N_C, number of gate drivers N_{GD}, maximum output voltage V_{sMax}, maximum blocking voltage (*MBV*) and peak value of CMV_{peak}.

Taking EV applications into account, several points on the torque-speed plane were considered for evaluating the THDv and efficiency, as summarized in Table 5.12. Since it was impractical to experimentally validate all the considered topologies, the alternative configurations were evaluated using PSIM simulations. The reliability of this comparative approach is firmly substantiated by the excellent agreement between the simulated and measured outcomes of the proposed system, which fully validates the accuracy of the software model used for the overall analysis.

Table 5.10 Cost of power devices (Infineon).

Device	Parameters	Unity cost
SiC MOSFET-IMBG120R034M2HXTMA1	1200V, 43A	9.46€
SiC MOSFET-IMBG65R026M2H	650V, 49A	10.72€
GaN HEMTs, GS66516B	650V, 47A	41.71€
Si-IGBTs-NXH40T120L3Q1PTG	1200V, 40A	7€
Si-IGBTs-IKZA40N120CS7	1200V, 56A	7.13€
Si-IGBTs-IKW40N65ET7XKSA1	650V, 49A	4.71€
Si Diode-IDP30E120	1200V, 50A	3.11€
Si Diode-IDWD40E65E7	650V, 49A	3.7€
SiC Diode-IDW40G120C5B	1200V, 40A	10.6€
SiC Diode-IDW40G65C5	650V, 40A	12.43€
Si MOSFET-IPW60R031CFD7XKSA1	600V, 40A	10.18€
Gate drive 1EDI60N12AF	isolated	1.91€
Isolated DC-DC converter NMH0515SC	±15Vout	12.8€
DC link capacitor-EKHU501VSN861MA60S	860µF, 500V	15€

Table 5.11 Comparisons in terms of components, cost, MBV and CMV.

Top	N_L	N_{sw-Si}	N_{sw-SiC}	N_{sw-GaN}	N_{d-Si}	N_{d-SiC}	N_C	N_{GD}	$\frac{V_{omax}}{V_{DC}}$	$\frac{MBV}{V_{DC}}$	$\frac{CMV}{V_{DC}}$	Cost [€]
A	2	6	\	\	6	\	1	6	0.5	1	0.5	164
B	2	\	6	\	\	6	1	6	0.5	1	0.5	223
C	3	12	\	\	6	\	2	12	0.5	0.5	0.5	329
D	3	\	\	12	\	6	2	12	0.5	0.5	0.5	877
E	3	12	\	\	12	\	2	12	0.5	1	0.5	318
F	3	\	12	\	\	12	2	12	0.5	1	0.5	465
G	3	\	6	6	\	6	2	12	0.5	1	0.5	624
H	3	\	\	12	\	\	2	12	0.5	0.5	0.5	707
I	6	18	\	\	\	\	3	18	0.65	1	0.32	505
L	6	12	\	6	12	\	3	18	0.65	1	0.32	645

Table 5.12 Comparisons in terms of efficiency and THD_v.

ω_r/ω_b / Top.	η (100%Load)				THD_v (100%Load)			
	0.25	**0.5**	**0.75**	**1**	**0.25**	**0.5**	**0.75**	**1**
A	88.1	88.8	88.9	90.7	26.2	25.2	24.2	23.2
B	92.4	93.4	93.6	95.5	24.1	23	22.2	21
C	93.3	94.1	94.6	96.2	16.3	15	14.1	13
D	97.1	98	98.2	99	16.3	15.3	14.3	13.2
E	93.1	94.1	94.6	96	16.5	15.1	14.2	13.1
F	96.8	97.7	97.9	98.7	16.4	15.1	14.1	13.3
G	97.1	98.1	98.5	99.1	16.3	15.5	14.5	13.2
H	97.2	98.1	98.5	99.1	16.4	15.2	14.2	13.3
I	96.9	97.3	97.8	98.3	7.8	7.15	6.7	6.3
L	97.8	98	98.8	99	7.8	7.1	6.8	6.2
	η (50%Load)				THD_v (50%Load)			
	0.25	**0.5**	**0.75**	**1**	**0.25**	**0.5**	**0.75**	**1**
A	89.3	90.1	90.2	90.5	26.2	25.2	22.4	22.2
B	93.3	94.3	94.4	94.9	24.1	23.1	21.9	21.8
C	94.4	95.4	95.5	95.8	16.3	15	10.5	10.3
D	97.4	98.4	98.5	98.9	16.3	15.3	10.6	10.3
E	96.1	95.2	95.3	95.6	16.5	15.1	10.6	10.2
F	97.1	98.2	98.2	98.5	16.4	15.1	10.7	10.4
G	97	98.1	98.2	98.9	16.3	15.5	10.8	10.2
H	97	98.1	98.1	98.9	16.4	15.2	10.8	10.1
I	97.1	97.9	97.9	98	7.8	7.1	6.9	7
L	98.1	98.7	98.7	98.9	7.8	7.1	6.9	7

The load torque was set to 50% and 100% of the rated value, while the operating speeds were selected as *0.25, 0.5, 0.75, 1.0, 1.25, 1.5,* and *2* times the base speed ω_b. The motor can deliver the rated torque up to the base speed. For higher speeds (*1.25, 1.5*, and $2\omega_b$), operation takes place in the FW region. As not all topologies were built in physical form, the data used for comparison were obtained through simulations conducted in PSIM. The consistency of this approach was validated by comparing the simulation data with experimental ones obtained using the implemented topologies. The results showed a high level of agreement, as illustrated in Fig. 5.28. Efficiency, THD_v, and CMV were evaluated across topologies. First, the distribution of conduction and switching losses across the various topologies was determined, as shown in Fig. 5.29. As expected, Topology A (all-silicon) had the lowest efficiency in all operating points, while using SiC in Topology B reduced losses significantly. Multilevel topologies C-L showed higher efficiency; Topologies D, G, and H (full WBG) reached 99% at rated torque but are costly. Topology L also achieved 99% efficiency at rated torque, thanks to low 3LI switching losses and GaN performance. Compared to Topology I, L shows a 0.7% gain in efficiency due to the absence of reverse recovery losses in GaNs. Topology L offers lower THD_v (6.2% *vs.* 13.2% of H), reduced CMV, and similar cost to G in all operating points, with better overall performance and reduced mechanical and EMI issues. Topologies D and H remain the most expensive due to full-GaN implementation.

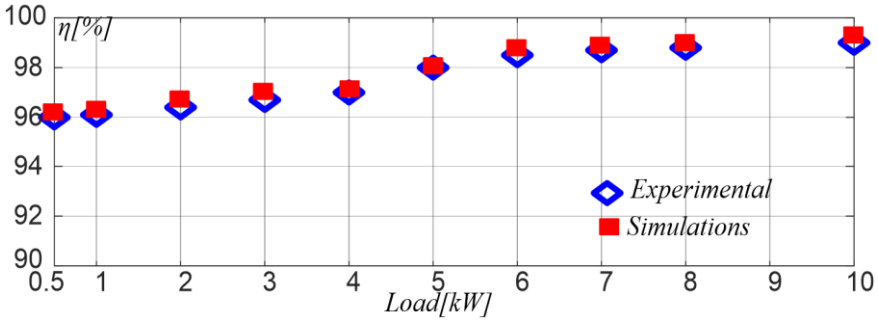


Fig.5.28 PSIM Simulations and experimental results. Efficiency of the propose Mixed Si-GaN inverter versus load at ωr=157rad/s, VDC2=250V, fsw=50kHz.

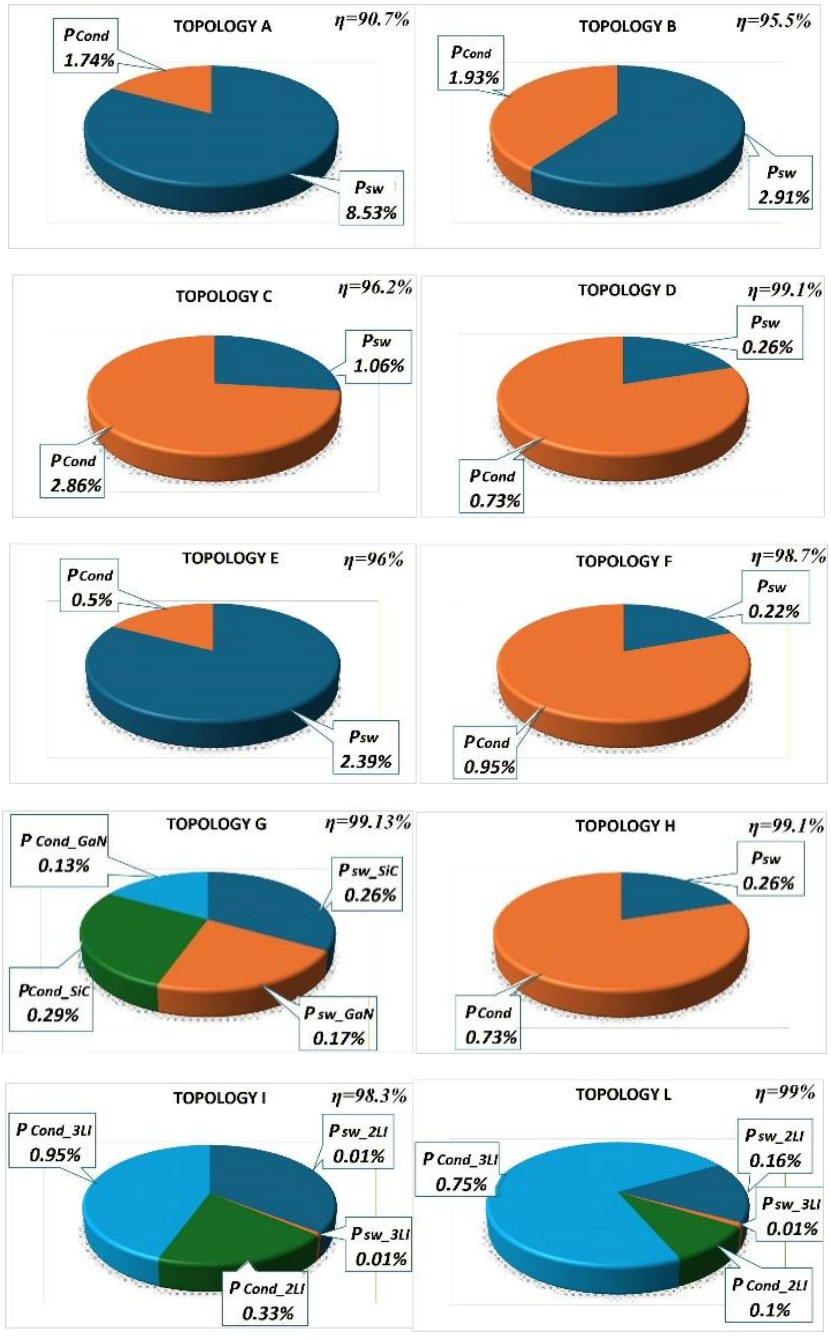


Fig. 5.29 Power losses distribution in all topologies at ω_r=157rad/s, V_{DC2}=250V, f_{sw}=50kHz.

Although the proposed topology employs a significantly larger number of components than the traditional 2LI topology, inevitably increasing both the overall system cost and the probability of failures, it achieves a higher efficiency and provides a more effective solution for EV applications. On the other hand, the proposed topology achieves higher efficiency with fewer power devices compared to an MLI delivering the same number of voltage levels. Furthermore, cooling requirements are reduced by using GaN devices on the 2LI and by operating the Si-IGBTs of the 3LI at a very low frequency, which almost completely eliminates switching losses. Furthermore, MLIs inherently reduce the CMV, thereby improving EMC performance.

5.9 CONCLUSIONS.

This chapter presented the design and development of a hybrid multilevel inverter for EV applications employing an OEW motor configuration. The proposed topology combines a three-level Si-IGBT T-type inverter operating at the full DC-link voltage with a GaN based two-level auxiliary inverter working essentially as an active filter. This architecture allows for the use of commercially available *650V* GaN devices in high-voltage EV systems (*800–1000V*). The experimental validation has shown several key benefits of the proposed solution. First, six-level output phase voltages with around 50% lower THDv compared to traditional structures, leading to reduced torque ripple and improved current and voltage waveforms. Second, a lower common-mode voltage is achieved, which reduces electromagnetic interference and bearing currents. Third high efficiency is obtained thanks to the synergetic use of GaN devices at moderate switching frequency (*50kHz*) and Si-IGBT at very low switching frequency. Furthermore, when considering only the active semiconductor devices in the economic evaluation, the proposed inverter maintains a cost comparable to that of a standard three-level GaN-based topology, proving to be a compact and cost-effective alternative to conventional solutions. Overall, the proposed OEW converter is a promising solution for next-generation high-voltage EV powertrains, combining the strengths of silicon and GaN technologies to meet the demands of efficiency, reliability and performance in electric mobility. Future work will focus on assessing converter behaviour under fault conditions and evaluating its robustness in real driving scenarios.

5.10 REFERENCE LIST

[1] M. H. Mousavi, H. Moradi and K. Rouzbehi, "Transition of DC Link Voltage from 400V to 800V in Electric Vehicles: Performance, Trade-Offs, and Technical Insights," *2025 10th International Conference on Technology and Energy Management (ICTEM)*, Tabriz, Iran, Islamic Republic of, 2025, pp. 1-7, doi: 10.1109/ICTEM66196.2025.11063549;

[2] M. Hassani Sadi, Z. Sadeghi and J. Bauman, "A Comprehensive Review of Universal Fast-Charging Techniques for 400-V and 800-V Electric Vehicles," in *IEEE Access*, vol. 13, pp. 153212-153233, 2025, doi: 10.1109/ACCESS.2025.3603845;

[3] S. Dutta and J. Bauman, "An Overview of 800 V Passenger Electric Vehicle Onboard Chargers: Challenges, Topologies, and Control," in *IEEE Access*, vol. 12, pp. 105850-105864, 2024, doi: 10.1109/ACCESS.2024.3435463;

[4] S. Dutta and J. Bauman, "An Overview of 800 V Passenger Electric Vehicle Onboard Chargers: Challenges, Topologies, and Control," in *IEEE Access*, vol. 12, pp. 105850-105864, 2024, doi: 10.1109/ACCESS.2024.3435463;

[5] Y. Zhou *et al*., "Overview of Medium Voltage SiC Power Module Packaging Technologies: Layout, Insulation, and Cooling Structure," in *IEEE Open Journal of Power Electronics*, vol. 7, pp. 249-266, 2026, doi: 10.1109/OJPEL.2025.3647112;

[6] E. E. Abramushkina, M. A. Frikha, B. Verbrugge, O. Hegazy and M. E. Baghdadi, "An Acceleration Approach for Real-Time Losses Calculation Model of Si IGBT and SiC MOSFET Traction Inverter Systems," in *IEEE Access*, vol. 14, pp. 41380-41397, 2026, doi: 10.1109/ACCESS.2026.3671183;

[7] H. Zhang *et al*., "GaN Power Devices for Electrified Transportation: Status, Challenges, and Perspectives," in *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2026.3656259;

[8] A. Poorfakhraei, M. Narimani and A. Emadi, "A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends," in *IEEE Open Journal of Power Electronics*, vol. 2, pp. 155-170, 2021, doi: 10.1109/OJPEL.2021.3063550;

[9] Foti, Salvatore, Antonio Testa, Salvatore De Caro, Luigi Danilo Tornello, Giacomo Scelba, and Mario Cacciato. 2021. "Multi-Level Multi-Input Converter for Hybrid Renewable Energy Generators" *Energies* 14, no. 6: 1764. https://doi.org/10.3390/en14061764;

[10] S. De Caro *et al*., "Motor Overvoltage Mitigation on SiC MOSFET Drives Exploiting an Open-End Winding Configuration," in *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11128-11138, Nov. 2019, doi: 10.1109/TPEL.2019.2902254;

[11] S. Foti, T. Scimone, A. Oteri, G. Scelba and A. Testa, "A reduced switch count, self-balanced,13-level inverter based on a Dual T-Type configuration," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2023.3281679;

[12] V. T. Somasekhar, M. R. Baiju, K. K. Mohapatra and K. Gopakumar, "A multilevel inverter system for an induction motor with open-end windings," *IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02*, Seville, Spain, 2002, pp. 973-978 vol.2, doi: 10.1109/IECON.2002.1185404;

[13] Y. Wang, D. Panda, T. A. Lipo and D. Pan, "Open-Winding Power Conversion Systems Fed by Half-Controlled Converters," in *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2427-2436, May 2013, doi: 10.1109/TPEL.2012.2218259;

[14] S. Foti *et al*., "An Open-End Winding Motor Approach to Mitigate the Phase Voltage Distortion on Multilevel Inverters," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2404-2416, March 2018, doi: 10.1109/TPEL.2017.2695244.;

[15] Z. Dong, Y. Liu, R. Huang and C. Liu, "Comparative Study on Topologies of Three-Level and Open-Winding Converters for PMSM Drives," *2021 IEEE 1st International Power Electronics and Application Symposium (PEAS)*, Shanghai, China, 2021, pp. 1-5, doi: 10.1109/PEAS53589.2021.9628577;

[16] S. Foti, A. Testa, G. Scelba, S. De Caro and L. D. Tornello, "A V2G Integrated Battery Charger Based on an Open End Winding Multilevel Configuration," in *IEEE Open Journal of Industry Applications*, vol. 1, pp. 216-226, 2020, doi: 10.1109/OJIA.2020.3035851;

[17] G. Gohil, L. Bede, R. Teodorescu, T. Kerekes and F. Blaabjerg, "Optimized Integrated Harmonic Filter Inductor for Dual-Converter-Fed Open-End Transformer Topology," in *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1818-1831, March 2017, doi: 10.1109/TPEL.2016.2562679;

[18] F. A. d. C. Bahia, C. B. Jacobina, N. Rocha, I. R. F. M. P. da Silva and R. P. R. de Sousa, "Hybrid asymmetric cascaded multilevel inverters based on three- and nine-level H-bridges," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 2017, pp. 1479-1486, doi: 10.1109/ECCE.2017.8095965;

[19] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath and C. A. Teixeira, "The Benefits of SiC mosfets in a T-Type Inverter for Grid-Tie Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2808-2821, April 2017, doi: 10.1109/TPEL.2016.2582344;

[20] K. Kumari, S. Mapa and R. Maheshwari, "Loss Analysis of NPC and T-Type Three-Level Converter for Si, SiC, and GaN based Devices," *2020 IEEE 9th Power India International Conference (PIICON)*, Sonepat, India, 2020, pp. 1-6, doi: 10.1109/PIICON49524.2020.9112873;

[21] Hasan Komurcugil, Sertac Bayhan, “Chapter 2 - Neutral-point-clamped and T-type multilevel inverters,” Editor(s): Ersan Kabalcı, Multilevel Inverters, Academic Press, 2021, Pages 29-56, ISBN 9780128216682, https://doi.org/10.1016/B978-0-12-821668-2.00003-9;

[22] S. S. Hakami, S. A. Q. Mohammed, L. M. Halabi, M. Kassas, M. M. AlMuhaini and M. A. Abido, "Common-Mode Voltage Reduction in Three-Level T-Type Converters Using a Quadruple Reference Voltage-Based PWM Technique," in *IEEE Open Journal of Power Electronics*, vol. 7, pp. 736-748, 2026, doi: 10.1109/OJPEL.2026.3663200;

[23] N. Bodo, E. Levi and M. Jones, "Investigation of Carrier-Based PWM Techniques for a Five-Phase Open-End Winding Drive Topology," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 2054-2065, May 2013, doi: 10.1109/TIE.2012.2196013;

[24] J. Kalaiselvi, et al., "Bearing Currents and Shaft Voltage Reduction in Dual-Inverter-Fed Open-End Winding Induction Motor With Reduced CMV PWM Methods," in IEEE Trans. on Ind. Electr., vol. 62, no. 1, pp. 144-152, Jan. 2015;

[25] G. Schoonhoven, et al., "MTPA- and FW-Based Robust Nonlinear Speed Control of IPMSM Drive Using Lyapunov Stability Criterion," in IEEE Trans. on Ind. Appl., vol. 52, no. 5, pp. 4365-4374, Sept.-Oct. 2016;

CHAPTER 6

Hybrid Si/WBG OEW converter for FACTS.

This chapter is extensively based on the following publication:

G. Baia et al., "A 36-kV 12-Mvar T-STATCOM Based on Mixed Si/WBG Open End Winding Multilevel Converter." 12-19. 10.1109/ICCEP65222.2025.11143704.

G. Baia et al., "A T-STATCOM converter structure synergistically combining IGBTs and SiC-MOSFETs." Electric Power Systems Research, Volume 255, 2026, 112835, ISSN 0378-7796, https://doi.org/10.1016/j.epsr.2026.112835.

6 HYBRID SI/WBG OEW CONVERTER FOR FACTS.

6.1 INTRODUCTION.

In the evolving energy landscape, system stability, reliability, and efficiency are becoming increasingly critical. The rapid growth of RES, the electrification of transportation, and the rising complexity of power grids have made voltage regulation and power quality more challenging. In Italy, the number of renewable energy plants seeking connection to the National Transmission Grid (RTN) has sharply increased, particularly in southern regions and on the islands, with around 90% of requests coming from plants with a capacity below *100MW* [1]. The current RTN connection standards require the construction of *150kV* bays, which are typically sized for larger plants. This leads to inefficient use of infrastructure and space, as well as additional regulatory complexity for smaller installations. To address these issues, Terna S.p.A. introduced a new *36kV* connection standard in 2021. This standard reduces costs, simplifies grid connections, and optimizes substation space by enabling multiple producers to share *36kV* bays, thereby facilitating renewable energy integration [1], as illustrated in Fig. 6.1.

Static synchronous compensators (STATCOMs) are key devices for improving grid stability, voltage regulation, and power quality through fast reactive power compensation. Since their introduction in the 1980s, STATCOMs have become integral components of modern transmission and distribution networks. They employ various semiconductor technologies, ranging from silicon-controlled rectifiers (SCRs), gate turn-off thyristors (GTOs), and Si-IGBTs to more recent WBG materials such as SiC and GaN [2], whose characteristics were discussed in detail in Chapter 2.

A comprehensive review of multilevel converter topologies, modulation methods, and control techniques for STATCOM applications is provided in [3]. The most common structures are summarized in Fig. 6.2. Distribution-type STATCOMs (D-STATCOMs) typically comprise a VSC, a DC energy storage device, and a coupling transformer. D-STATCOMs can be connected to the MV distribution or MV industrial load bus either directly, or via a step-up, semi-custom coupling transformer [4], as shown in Figs. 6.2a and 6.2b respectively.

Transmission-type STATCOMs (T-STATCOMs) serving HV transmission systems, are generally based on MLCs, coupled with transformers, reactors, and control systems, [5-7], as in Fig. 6.2c.

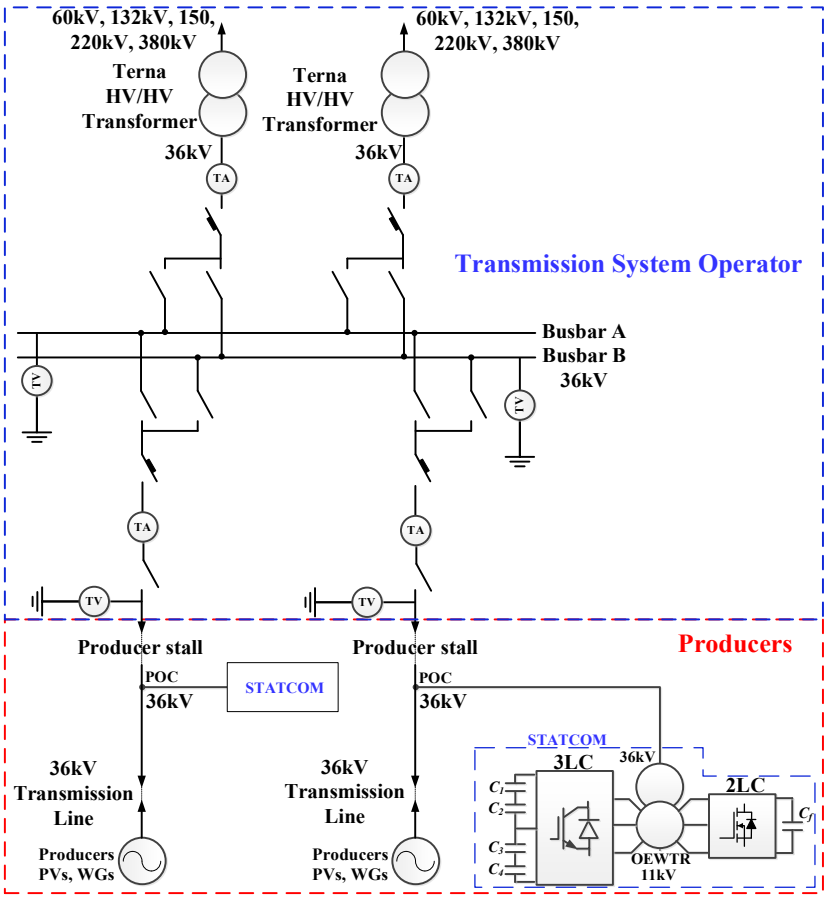


Fig. 6.1 Block diagram of the proposed Mixed Si/SiC OWMTS for the new 36kV connection standard.

There are four topologies that are the most commonly used for the multilevel STATCOM applications. These are cascaded multilevel converters (CMC), NPC, FC and MMC [8-11]. A detailed comparison among these topologies in STATCOM application has been done in [12]. Among these CMC is widely used for STATCOM applications due to its modularity but suffers dc-link capacitor voltages equalization problems [13], requirement of additional series filter reactance [14] and requires complex control for fault operation [15]. The MMC topology offers benefits such as modularity, reliability, and high voltage levels

but has drawbacks including increased power losses, stress on switching devices, a high number of modules, and submodule capacitor voltage ripple [16].

T-STATCOM usually deploy CMC or MMC based solutions but that may not be the best choice and suitable for smaller-rated STATCOMs, as fewer cascaded cells require higher switching frequencies, leading to increased losses which demand other solution. Hybrid multilevel converters seems a viable solution as proposed in [17-18]. Some hybrid solutions involved cascaded H-bridge and full-bridge neutral point clamped inverter [19] or using diode-clamped modular multilevel converter [20].

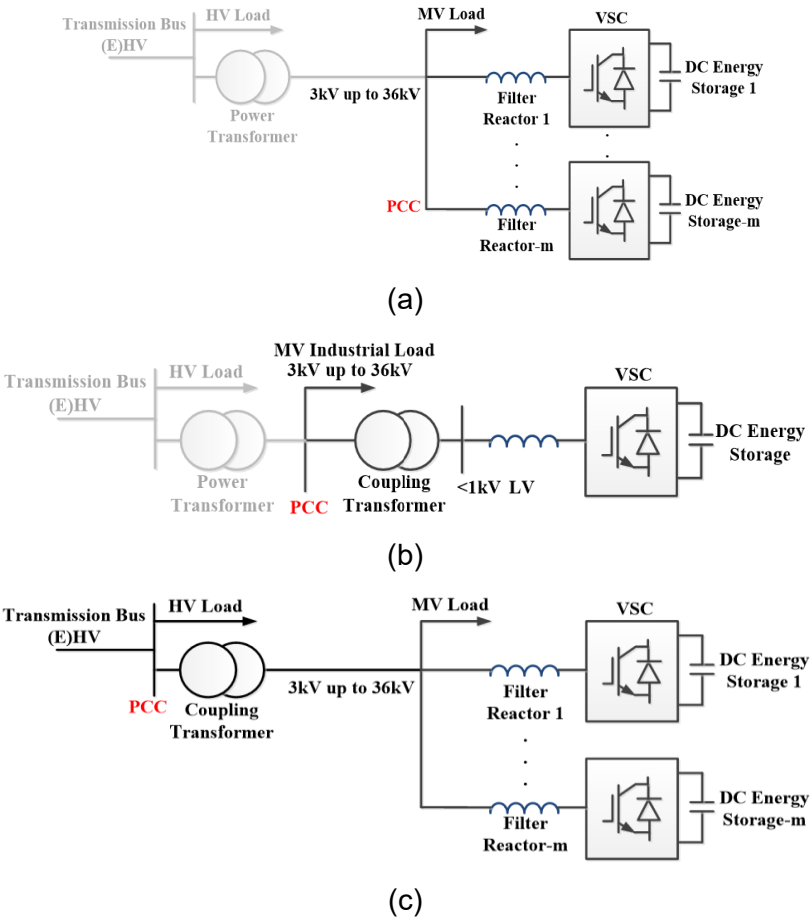


Fig.6.2 Block diagrams of STATCOM systems with VSCs. (a) D-STATCOM, (b) D-STATCOM with coupling transformer, (c) T-STATCOM.

Si/WBG hybrid approaches have been explored in [21] and [22]. Accordingly, a selective harmonic cancellation strategy was adopted, reducing the required DC-link voltage and improving efficiency. This approach is more cost-effective than conventional CMC-based T-STATCOMs fully implemented with SiC-MOSFETs, while achieving comparable efficiency. For example, [22] introduces a topology combining a three-level NPC inverter using Si-IGBTs with a high-frequency CHB converter employing SiC devices, where the CHB stage handles harmonic filtering while the NPC inverter operates with reduced switching losses. In [23], a CHB-based system is described in which low-frequency Si-IGBT cells and high-frequency SiC cells operate together, using selective harmonic cancellation to lower the DC-link voltage and enhance efficiency. Based on this concept, an OEW-based converter geared towards T-STATCOM applications, has been developed which combines Si-IGBT and SiC-MOSFET to achieve a favorable compromise between component cost and performance. For a target application at *154kV*, the proposed system comprises a three-level NPC converter (3LC) and a two-level SiC-based converter (2LC), connected to the secondary side of an OEW coupling transformer (OEW-CTR), as in Fig. 6.3. In addition to the hybrid Si/WBG approach, the proposed topology introduces two key features. First, the 2LC ensures harmonic filtering in compliance with IEEE Std. 519-2014. Second, active balancing of the 3LC DC-link capacitors is achieved through a switching-angle control strategy. The proposed system targets only low-order harmonics (up to the 19th), thereby reducing both voltage and power losses while remaining within IEEE Std. 519-2014 limits. Finally, current limitations in voltage and power ratings makes GaN unsuitable for transmission-level STATCOMs, where the proposed SiC-based solution remains the more practical and viable choice.

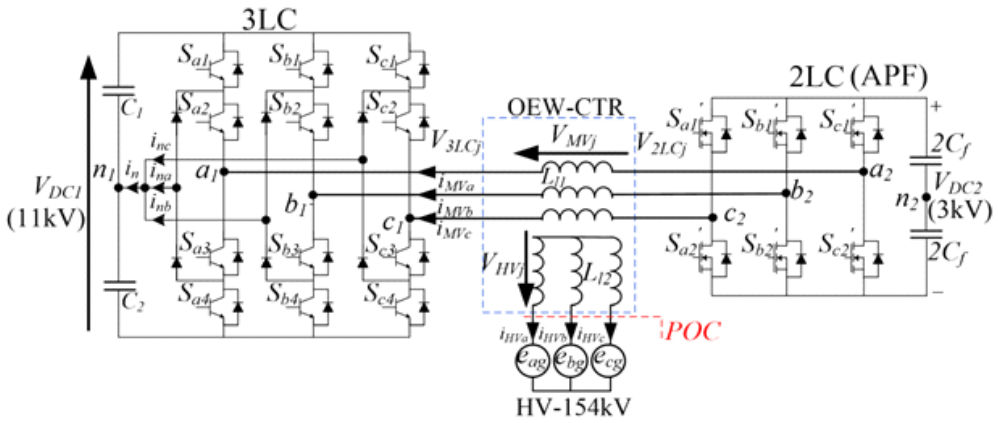


Fig.6.3 Proposed Si/WBG MOSFET OEW T-STATCOM.

6.2 WORKING PRINCIPLES.

The developed converter encompasses an OEW-CTR, a 3LC and a 2LC. The 3LC contains twelve Si-IGBTs (S_{ji}), six clamping diodes (D_{ji}) and two capacitors C_1, C_2, while the 2LC encompasses six SiC-MOSFETs ($S_{ji}^{'}$) and a capacitor C_f with $j=a,b,c$, $i=1,2,3,4$ and $i^{'}=1,2$. The DC buses of the two converters are not connected to each other. This prevents zero-sequence currents (ZSCs) from occurring and allows two different DC bus voltages, $V_{DC1}=11kV$ and $V_{DC2}=2.7kV$, to be set. The 3LC uses *6.5kV* Si-IGBT modules, while the 2LC is equipped with *3.3kV* SiC-MOSFET modules. According to Fig. 6.3, the AC transformer secondary *j*-phase voltage $V_{MVj}(t)$ is given by composition of the output voltages of the 3LC and 2LC converters, denoted as $V_{3LCj}(t)$ and $V_{2LCj}(t)$ and the differential voltage $V_0(t)$:

$$V_{MVj}(t) = V_{3LCj}(t) - V_{2LCj}(t) + V_0(t) \tag{47}$$

The voltage $V_0(t)$, established between the midpoints n_1 and n_2 of the DC buses of the two inverters, is given by [24]:

$$V_0 = \frac{1}{3}(V_{3LCa} + V_{3LCb} + V_{3LCc} - V_{2LCa} - V_{2LCb} - V_{2LCc}) \tag{48}$$

The voltage across the phase terminal j_1 of the 3LC, and the mid-point n_1, may take three levels:

$$V_{3LCj} = \frac{l' - 1}{2} V_{DC1} \quad l' = 0, 1, 2. \tag{49}$$

being V_{DC1} the total DC-Bus voltage of the 3LC. The voltage across the phase terminal j_2 of the 2LC and the mid-point n_2 of the DC-bus V_{DC2}, may take two levels:

$$V_{2LCj} = \frac{2l'' - 1}{2} V_{DC2} \quad l = 0, 1 \tag{50}$$

By replacing (48) and (50) into (47), the AC transformer secondary phase voltage $V_{MVj}(t)$ becomes:

$$V_{MVj}(t) = \frac{l' - 1}{2} V_{DC1} - \frac{2l'' - 1}{2} V_{DC2} + V_0 \tag{51}$$

According to (51), the waveform $V_{MVj}(t)$ and in particular the number of voltage levels N_L depends on the DC bus voltages ratio $k_v=V_{DC2}/V_{DC1}$, as shown in Table 6.1.

Table 6.1 Voltage Levels V.S. K_v

k_v	N_L
1	5
$0.5<k_v<1$; $k_v<0.5$	6
0.5	4

An optimal selection of the voltage ratio k_v is of paramount importance. For a given V_{DC1}, a higher k_v increases the voltage stress on the power devices of the 2LC and raises the switching losses. On the other hand, choosing a low value of k_v deteriorates the waveform of the transformer secondary current and leads to higher power losses. To minimize switching losses, the 3LC employs a line-frequency Step Modulation with a single switching angle α, while the 2LC is PWM operated using a conventional Space Vector approach. A relatively low switching frequency is chosen for the SiC-MOSFET devices, yet it is sufficient to suppress voltage harmonics up to the *19th* order while maintaining very low switching losses. The main tasks assigned to the 3LC are grid synchronization, regulation of the 3LC DC bus voltage, and equalization of V_{C1} and V_{C2}. In contrast, the 2LC is responsible for voltage harmonics cancellation, reactive power regulation, and regulation of the 2LC DC bus voltage.

6.2.1 Grid synchronization.

The 3LC is driven through a single switching angle, which is given by:

$$\alpha = cos^{-1}\left(\frac{2V_{DC1}}{\pi \hat{V}_{13LCj}}\right) \tag{52}$$

where $\hat{V}_{13LCj}{}^{*}$ is the peak value of the fundamental component V_{13LCj} of the *j*-phase voltage. Switching rules for the devices of the pole *a* are listed in Tab. 6.2.

Table 6.2 3LC Pole voltage switching rules.

θ_e	I'	V_{3LCa}	On	Off
$0<\theta_e<\alpha$; $\alpha<\theta_e<\pi+\alpha$; $2\pi-\alpha<\theta_e<2\pi$	1	0	S_{a2}, S_{a3}	S_{a1}, S_{a4}
$\alpha<\theta_e<\pi-\alpha$	2	$V_{DC1}/2$	S_{a1}, S_{a2}	S_{a3}, S_{a4}
$\pi+\alpha<\theta_e<2\pi-\alpha$	0	$-V_{DC1}/2$	S_{a3}, S_{a4}	S_{a1}, S_{a2}

Grid synchronization is achieved by considering the actual angular position θ_g of the grid voltage vector V_{HV} in determining the switching instants [25]. Waveforms of V_{3LCj} and V_{13LCj} are shown on Fig. 6.4. Similar rules can be derived for the devices of the other two poles.

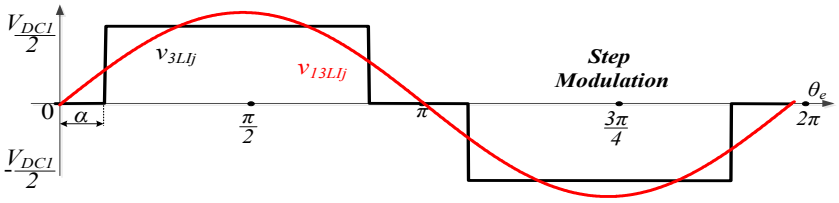


Fig. 6.4 3LC output voltage and fundamental component waveforms.

6.2.2 3LC DC-Bus voltage regulation.

According to (52), the 3LC operates at a constant switching angle, because at steady state both $V_{DC1}$and $\hat{V}_{13LCj}{}^{*}$are constant. Hence, the only means to adjust the active power absorbed by the 3LC in order to control V_{DC1} is to act on the phase displacement *d* between the grid phase voltage vector V_{HV} and the transformer secondary phase voltage vector V_{MV}. In fact, by neglecting the series resistance of the coupling transformer, the real power P which is absorbed at steady state by the converter, is given by:

$$P = \frac{V_{HV} t_r V_{MV}}{3X_L} \sin(\delta) \approx \frac{V_{HV} t_r V_{MV}}{3X_L} \delta \qquad (53)$$

where X_L represents the total leakage reactance of the coupling transformer at the primary side and t_r is the transformer turn ratio, while V_{HV} is the rms line-to-neutral primary voltage and V_{MV} the rms line-to-neutral secondary voltage. In practice, P is very small, being equal to the power losses in the two inverters, resulting in a close to zero (<2°) angle δ, Fig. 6.5.

Hence, an angle δ is subtracted to the angular position θ_g of the grid voltage vector V_{HV} to determine the switching instants through the rules listed in Tab.6.2. This angle is computed as:

$$\delta = atan\left(-\frac{P_{3LC}}{Q_{3LC}}\right) \qquad (54)$$

being Q_{3LC} the 3LC output reactive power and P_{3LC} the composition of the real power absorbed at steady state by the 3LC converter and the power required to keep constant V_{DC1}, which in practice is provided by a closed-loop control system.

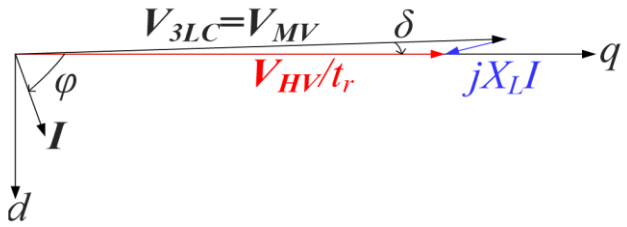


Fig. 6.5 Voltage and current vectors in the qd-axes system.

6.2.3 3LC DC-Link voltage equalization.

Control of the total 3LC DC-link voltage V_{DC1} is not sufficient, as it is also necessary to equalize the voltage across the two DC-bus capacitors C_1 and C_2. According to Fig. 6.6, by assuming C_1=C_2=C, the voltage V_2 is given by:

$$V_2 = \frac{1}{C}\int_0^T i_n dt \qquad (55)$$

where T is the fundamental period of the grid voltage and i_n the neutral current.

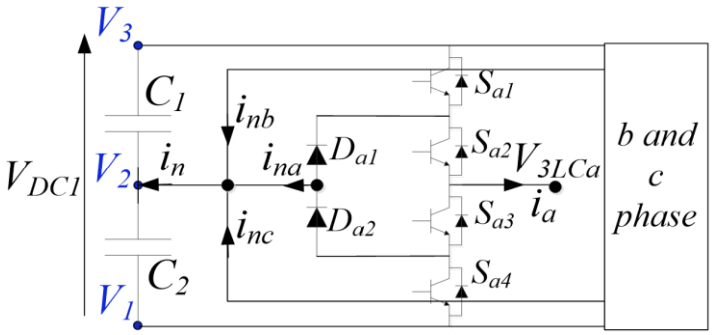


Fig. 6.6 3LC DC-Link.

According to (55), V_2 can be kept equal to $0.5V_{DC1}$ by controlling the mean value of the current i_n circulating through the midpoint n_1 of the 3LC DC-link. The current i_n is given by composition of the midpoint currents i_{na}, i_{nb} and i_{nc}:

$$i_n = i_{na} + i_{nb} + i_{nc} \qquad (56)$$

As is shown in Fig. 6.7, a small corrective term *γ* is added to the switching angle *α* to adjust the ratio between the width of positive and negative pulses of i_n. The average value of i_n in a fundamental period *T* of the grid voltage, is then given by:

$$\bar{\imath}_n = \frac{3I}{\pi}[\sin(\alpha+\gamma) - \sin(\alpha-\gamma)] \quad (57)$$

being *I* the magnitude of the current vector *I*. The corrective term *γ* is in practice generated by a voltage control loop processing the difference between V_{C1} and V_{C2}.

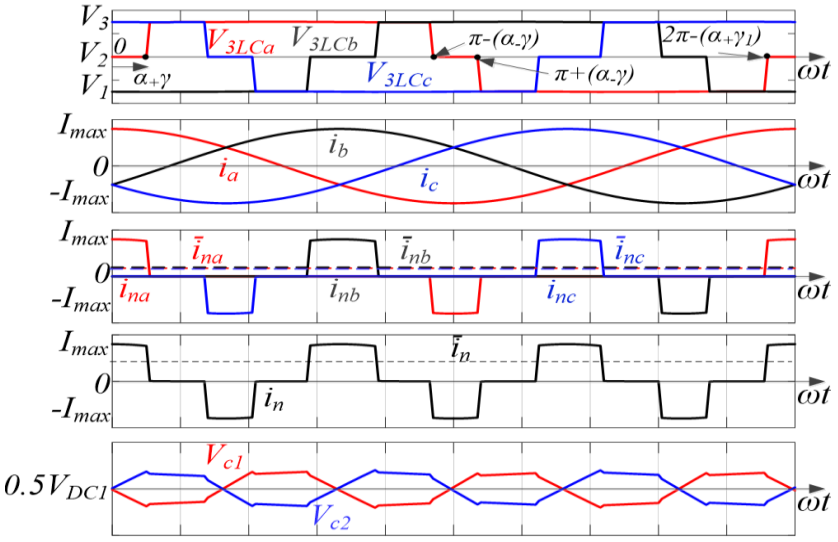


Fig. 6.7 Equalization of 3LC DC bus capacitors voltages.

6.2.4 Voltage harmonics cancellation.

According to a Fourier series expansion the 3LC output phase voltage $V_{3LCj}(t)$ can be written as:

$$V_{3LCj}(t) = V_{13LCj}(t) + \sum_{h=5}^{Nmax} V_{h3LCj}(t) \quad (58)$$

where *h>1*, odd and not multiple of *3*, while N_{max}=+∞.

The peak value of the fundamental component V_{13LCj} of $V_{3LCj}(t)$ is given by:

$$\hat{V}_{13LCj} = \frac{2V_{DC1}}{\pi}cos(\alpha) \quad (59)$$

The peak value of the generic *h*-order harmonic $V_{h3LCj}(t)$ caused by the line frequency commutation of the 3LC is:

$$\hat{V}_{h3LCj} = \frac{2V_{DC1}}{h\pi}\cos(h\alpha) \tag{60}$$

To achieve a transformer secondary voltage $V_{MVj}(t)$ with a sinusoidal waveform, all the harmonics $V_{h3LCj}(t)$ caused by step modulation must be compensated by the 2LC acting as an active filter. However, in practice, harmonics of order higher than the 50^{th} are not considered by IEEE Std. 519-2014, thus can be neglected. For given V_{DC1}, the peak value of the generic harmonic term $V_{h3LCj}^{*}(t)$ is function of the switching angle *a*. Therefore, the minimum value of V_{DC2} required to cancel a given set of harmonics changes with *a*, in turn affecting the value of k_v. In Fig. 6.8 the voltage ratio k_v and the THD_v of $V_{MVj}(t)$ (computed up to the 50^{th} harmonic), are plotted versus α when cancelling different sets of harmonics. These sets are identified by the order of the highest harmonic eliminated N_{max}. As expected, a zero THD_v across all values of α is achieved when $N_{max}=+\infty$. However, in this case, the maximum value of k_v approaches *0.5*, meaning that the 2LC DC bus voltage must be at least half that of the 3LC. It can be also observed that a THD_v close to zero can be achieved with $N_{max}= 19$, with $\alpha<20°$ and *0.25* k_v, leading to a 2LC DC bus voltage equal to only 25% that of the 3LC. In this condition, the harmonic component of the 3LC output phase V_{H3LCj} to be compensated is in practice given by:

$$V_{H3LCj}(t) = \sum_{h=5}^{19} V_{h3LCj}(t) \tag{61}$$

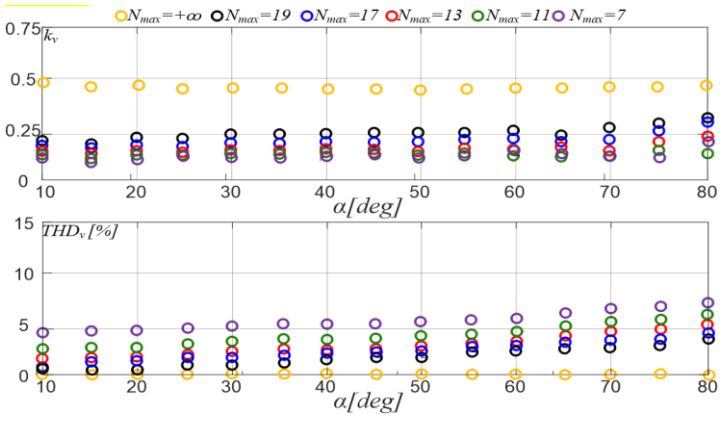


Fig. 6.8 Voltage ratio K_v vs. mx and N_{max}.

The 2LC is driven in order to compensate for the component $V_{H3LCj}(t)$. Hence, a term of the 2LC reference voltage $V_{2LCj}^{*}(t)$ is set equal to $V_{H3LCj}(t)$. In these conditions, as shown in Fig. 6.9, the peak value of $V_{H3LCj}(t)$ takes its minimum value ($0.116V_{DC1}$) for $\alpha_{opt}=15°$, as well as k_v and THD_v reaching 0.232 and 0.47%, respectively. Therefore, the 3LC is voltage controlled in open-loop mode, keeping constant the switching angle at α_{opt}. This results in a constant output voltage $\hat{V}_{13LCj}$, which is set equal in practice to the transformer secondary voltage.

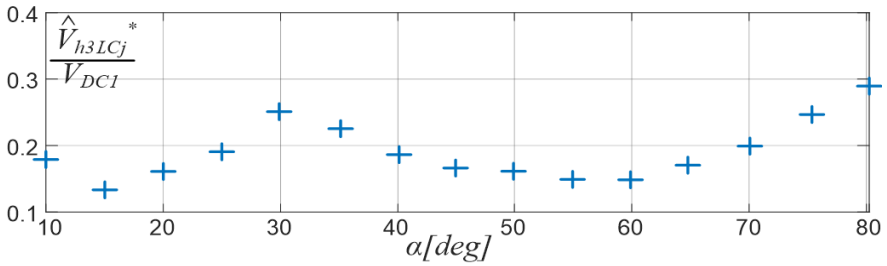


Fig. 6.9 Peak value of V_{H3LCj}'/V_{DC1} vs. α.

6.2.5 Reactive power regulation.

The T-STATCOM regulates the voltage at the point of connection (POC) through injection of reactive current. When the voltage at the POC falls below the rated value, the T-STATCOM feeds a negative reactive power to the grid, working in capacitive mode. Conversely, if the voltage at the connection point exceeds the rated value, the T-STATCOM supplies a positive reactive power, working in inductive mode. Assuming constant δ and V_{HV}, the reactive power can be adjusted by varying the transformer secondary voltage $V_{MVj}(t)$, because the reactive power Q is given by:

$$Q = V_{HV}\left[\frac{V_{HV}-t_r V_{MV}}{3X_L}\right]cos(\delta) \qquad (62)$$

The transformer secondary voltage $V_{MVj}(t)$ is in turn given by composition of the fundamental components of the output voltages of the two converters, V_{13LC} and V_{12LC}. The voltage V_0 across the midpoints of the two converters consists of only zero-sequence components and can be neglected in the reactive power calculation, giving:

$$Q = V_{HV}\left[\frac{\Delta V_L}{3X_L}\right]cos(\delta) \qquad (63)$$

$$\Delta V_L = V_{HV} + t_r(V_{12LC} - V_{13LC}) \quad (64)$$

Therefore, DV_L should be made negative to operate the T-STATCOM in capacitive mode, and positive DV_L to achieve inductive mode. The voltage DV_L and in turn the reactive power Q, is regulated by adjusting $V_{12LC}(t)$, because the magnitude of the fundamental component of the 3LC phase voltage is constant, being set to:

$$V_{13LC}(t) = V_{MV}(t) = \frac{V_{HV}(t)}{t_r} \quad (65)$$

6.2.6 2LC DC-Bus voltage regulation.

According to a dq reference system, with the d-axis aligned with the 2LC output voltage vector, the active power P_{2LC} absorbed by the 2LC and the output reactive power Q_{2LC} are:

$$P_{2LC} = \frac{3}{2}\left(V_{2LCcq} i_q + V_{2LCcd} i_d\right) \quad (66)$$

$$Q_{2LC} = \frac{3}{2}\left(V_{2LCcd} i_q - V_{2LCcq} i_d\right) \quad (67)$$

where V_{2LCcqd} are defined in the appendix. The reactive power Q_{2LC} is in practice forced to zero to minimize the power losses and the DC bus voltage, hence the voltage and current vectors are in phase, leading to:

$$i_d = \frac{2}{3}\frac{P_{2LC}}{V_{2LCcd}} = \frac{2}{3}\frac{P_{2LC}}{V_{2LC}} \quad (68)$$

$$i_q = 0 \quad (69)$$

Under these conditions, P_{2LC} and Q_{2LC} can be independently regulated by acting on the qd-axes components of the 2LC output current. As shown in Fig. 6.10 a *qd*-axis current control is used on the 2LC, where the DC bus voltage V_{DC2} is controlled through i_d while Q_{2LC} is kept null by acting on i_q. Then, the 2LC reference phase voltage is given by:

$$V^*_{2LCj}(t) = V^*_{H3LCj}(t) + V^*_{2LCcj}(t) \quad (70)$$

where $V^*_{H3LCj}(t)$ is responsible for elimination of voltage harmonics and $V^*_{2LCcj}(t)$ is determined by controlling the reactive power Q_{2LC} and the 2LC DC link voltage V_{DC2}.

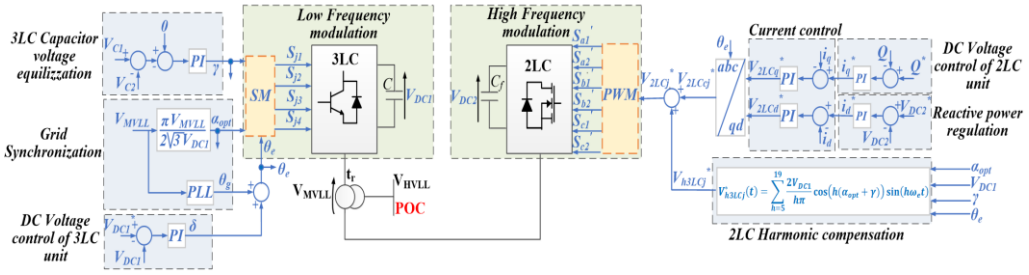


Fig. 6.10 Proposed control algorithm for the Mixed Si/WBG T-STATCOM.

6.3 BASIC CONVERTER DESIGN.

For a *154kV* T-STATCOM application, the value of k_v and the maximum current on the MV side of the coupling transformer must be first stated to determine the 3LC DC bus voltage V_{DC1} and the voltage rating of the Si-IGBT modules. According to the datasheet of the INFINEON FF2000UXTR33T2M1 SiC-MOSFET module, a maximum *800A* phase current is selected. Given this current, a *8.3kV* rms line-to-line V_{MVLL} voltage is chosen, to achieve an *8MVar* nominal reactive power. This leads to a transformer turns ratio:

$$t_r = \frac{V_{HVLL}}{V_{MVLL}} = \frac{154\ kV}{8.3\ kV} = 18.5 \qquad (71)$$

Moreover, a *6.8kV* peak-phase voltage $\hat{V}_{MV}$ is achieved which, for operation at α_{opt}=*15*°, (52) leads to:

$$V_{DC1} = \frac{\pi}{2}\frac{\hat{V}_{MV}}{cos(\alpha_{opt})} \approx 11kV \qquad (72)$$

The total reference phase voltage for the 2LC $V^*_{2LCj}(t)$ is shown in Fig. 6.11. It is given by the sum of two terms: one resulting from the cancellation of V_{H3LCj} harmonic components up to the *19*th order, and the other resulting from reactive power control $V_{2LCcj}(t)$.

$$V^*_{2LC}(t) = \sum_{h=5}^{19}\frac{2V_{DC1}}{h\pi}\cos(h15^o)\sin(h\theta_e) + V_{12LC}cos(\theta_e) \qquad (73)$$

From (63), (64) and (65), since *Q=8MVar*, V_{HVLL}=*154kV*, X_L=*363Ω* and t_r=*18.5*, it comes that:

$$\hat{V}_{12LCj} \approx 0.8kV \qquad (74)$$

It can be demonstrated in Fig. 6.11 that within a fundamental half-period, $V^{*}_{2LCj}(t)$ reaches its peak value at $\theta_e=90^{\circ}$, achieving $\hat{V}_{2LCj}{}^{*} \approx 1.4kV$. The minimum 2LC DC bus voltage required to generate *1.4kV* using the SVM technique is *1.4kV/0.577=2.4kV*. Therefore, *6.5kV*, *1kA*, Si-IGBT modules FZ1000R65KE4 and *3.3kV, 1kA*, SiC-MOSFET FF2000UXTR33T2M1 modules provided by Infineon are fully suitable.

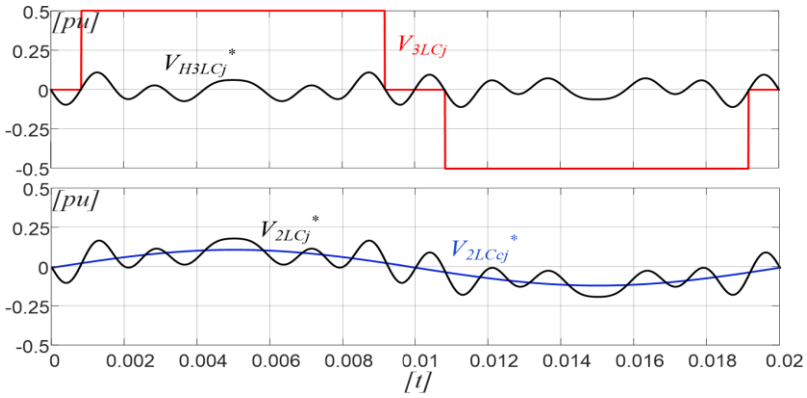


Fig. 6.11 Harmonics compensation and Q regulation.

6.4 SIMULATION ASSESSMENT.

The proposed converter was evaluated using PSIM and MATLAB/Simulink simulations. PI controllers were tuned using the automatic tuning tool provided by MATLAB/Simulink, achieving the parameters listed in Table 6.3. Main parameters of the simulated system are listed in Table 6.4.

Table 6.3 Gains of PI controllers.

3LC capacitor voltage equalization		**Reactive power regulation**	
Proportional gain	0.01	Proportional gain	0.2
Integral gain	0.5	Integral gain	4
DC voltage control of 3LC unit		**q-axis current control**	
Proportional gain	0.1	Proportional gain	15
Integral gain	1	Integral gain	150
DC voltage control of 2LC unit		**d-axis current control**	
Proportional gain	0.2	Proportional gain	15
Integral gain	4	Integral gain	150

Table 6.4 T-STATCOM Parameters.

3LC	
Rated power	±8MVAr
DC bus voltage	11kV
Energy stored in the DC bus capacitors	250kJ
DC bus capacitors	16 x 2kV 4.6mF
Switching frequency	50Hz
SI-IGBT Modules	12 x FZ1000R65KE4, 3.3kV, 1kA
Clamping diodes	6 x RBK86525XX-ND, 6.5kV, 2.5kA
2LC	
Rated RMS current	560A
DC bus voltage	2.7kV
Energy stored in the DC bus capacitors	62kJ
DC bus capacitors	4 x 2kV 4.6mF
Switching frequency	10kHz
SiC MOSFET Modules	3 x FF2000UXTR33T2M1, 3.3kV, 1kA
Harmonics cancelled	$5^{th} \div 49^{th}$
Coupling transformer	
Rated primary voltage	154kV
Rated secondary voltage	9kV
Rated power	12MVA
Total leakage reactance (HV side)	375Ω

The DC bus voltage of the 3LC is set to *11 kV*, whereas the DC link voltage of the 2LC is set to *2.7kV*. Figure 6.12 shows the response of the system to a step change in reference reactive power, resulting in a transition from capacitive to inductive mode at full power. The figure shows the MV and HV side currents, qd-axes currents, 3LC *a*-phase voltage, 2LC *a*-phase phase voltage, MV side *a*-phase voltage, 3LC DC bus capacitors voltages, DC Links of 3LC and 2LC, filtered *a*-phase MV voltage of the transformer V_{MVfa} and grid current i_{HVa}. The response time is under *2ms*, which is quite satisfactory for a T-STATCOM. Furthermore, stable voltages are established on both the 3LC and 2LC DC buses. The voltage THD_v at the POC is *0.7%,* fully complying with the IEEE Std. 519-2014 requirements (*<2.5%* for $69kV<V_{POC}<161kV$). Table 6.5 shows the percentage values of the amplitude of the phase voltage harmonics on the MV side at *+8MVar* versus the switching frequency.

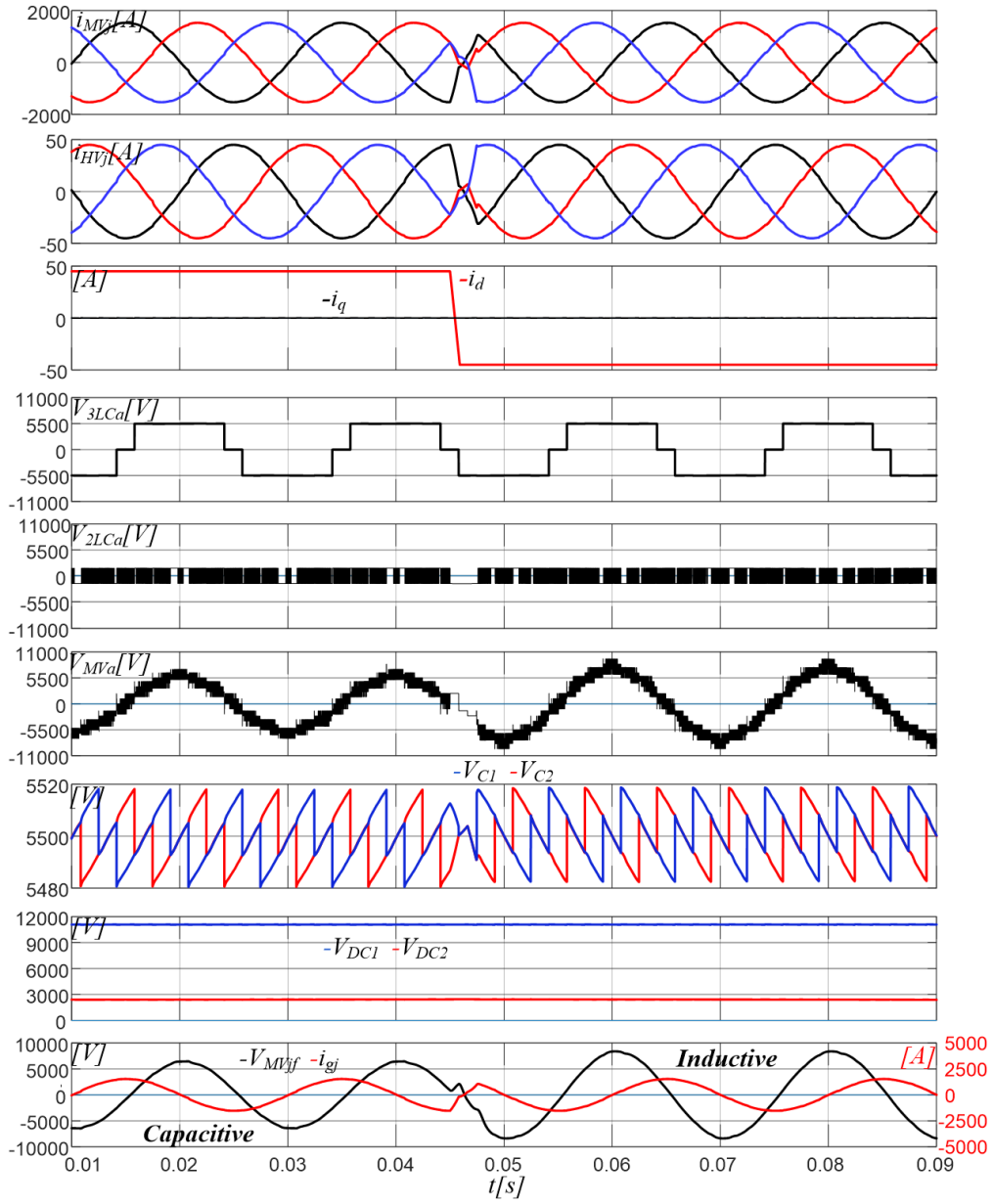


Fig. 6.12 Transition from capacitive to inductive mode at 8MVar. MV side currents i_{MVj}, HV side currents i_{HVj}, qd-axes currents i_{qd}, 3LC output voltage V_{3LCa}, 2LC output voltage V_{2LCa}, MV side phase voltage V_{MVa}, 3LC capacitors voltages V_{C1} and V_{C2}, V_{DC1},V_{DC2}, filtered MV phase voltage of V_{MVfa} and grid current i_{HVa}.

According to the IEEE Std. 519-2014 for high-voltage systems, each individual harmonic component must not exceed 1.5% of the fundamental while the THD_v at the POC must be lower than *2.5%.* A *10 kHz* switching frequency is sufficient to meet these requirements. Increasing the switching frequency beyond *10 kHz* would only be detrimental in terms of power losses.

Table 6.5 Percentage value of the amplitude of voltage harmonics on the MV side, and THD_v at POC vs. the Switching Frequency at 8 Mvar.

Harmonic order	2LC Switching frequency			
	500Hz	5kHz	10kHz	15kHz
5th	1.97	1.26	0.3	0.25
7th	18.85	1.4	0.24	0.2
11th	5.39	1.14	0.19	0.13
13th	5.65	1.7	0.2	0.2
17th	10.53	2.29	0.36	0.36
19th	2.15	1.17	0.23	0.22
23rd	1.37	0.17	0.1	0.1
25th	2.85	0.85	0.14	0.14
29th	1.39	0.39	0.19	0.11
31st	1.65	0.65	0.14	0.14
35th	1.53	0.53	0.16	0.16
37th	2.05	0.05	0.13	0.11
41st	1.19	0.19	0.19	0.12
43rd	0.65	0.35	0.14	0.11
47th	0.53	0.23	0.16	0.11
49th	1	0.1	0.13	0.1
THD_v @ POC	23%	4.1%	0.7%	0.69%

Table 6.6 deals with the amplitude of voltage and current harmonics on the HV side at *10kHz*, for both capacitive and inductive operation. It is worth emphasizing that while all harmonics up to the 49th order were analyzed, the proposed system eliminates only those up to the 19th, as subsequent higher-order harmonics are considered negligible. The ability of the system in equalizing the voltages across the two capacitors of the 3LC DC bus is illustrated in Fig. 6.13. At *t=0s*, a *200Ω* resistor is parallel connected to C_1 to create a voltage imbalance. At *t=0.1s*, the voltage equalization is enabled, promptly correcting the imbalance.

Table 6.6 Voltage and current harmonics on the HV side and THD at ±8 Mvar and 10kHz.

Harmonic order	Inductive Q=8MVar		Capacitive Q=-8MVar	
	V_{HVa}	i_{HVa}	V_{HVa}	i_{HVa}
5th	0.3	0.2	0.35	0.19
7th	0.24	0.14	0.24	0.2
11th	0.19	0.11	0.29	0.29
13th	0.2	0.13	0.2	0.12
17th	0.36	0.26	0.36	0.26
19th	0.23	0.13	0.23	0.33
23rd	0.1	0.09	0.1	0.2
25th	0.14	0.04	0.14	0.04
29th	0.19	0.09	0.29	0.19
31st	0.14	0.04	0.14	0.11
35th	0.16	0.06	0.16	0.16
37th	0.13	0.06	0.13	0.11
41st	0.19	0.09	0.19	0.06
43rd	0.14	0.04	0.14	0.03
47th	0.16	0.06	0.17	0.05
49th	0.13	0.03	0.14	0.03
THD	0.7%	0.45%	0.87%	0.5%

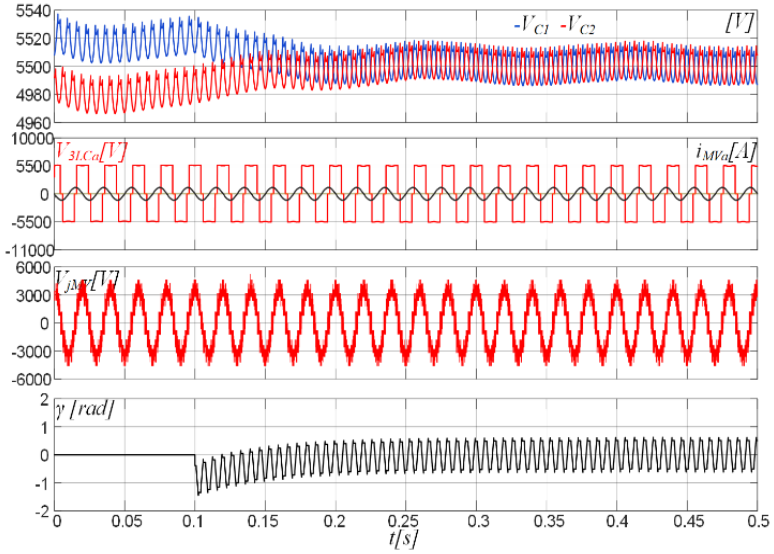


Fig. 6.13 3LC DC bus capacitors voltage equalization. 3LC capacitors voltages V_{C1} and V_{C2}, 3LC output voltage V_{3LCa}, MV side currents i_{MVa}, a-phase MV voltage of the transformer V_{MVa}, corrective term γ.

6.5 6 kVAR DOWNSCALED T-STATCOM PROTOTYPE.

Experimental tests were carried out on a scaled-down *6KVar* T-STATCOM converter, whose key features are illustrated in Tab. 6.7. The experimental system, shown in Fig. 6.14, is connected to a grid emulator through the coupling transformer. The control system is implemented on a dSPACE MicroLabBox 1260 DSP board. According to optimal design criteria, the switching angle α was set to *15°*. The *6kVA* scaled system operates with the same k_v*=0.26*, switching angle and switching frequency of the simulated system. The shape of the waveform of the 3LC output voltage is identical in both systems despite the different power ratings. Consequently, the percentage values of the amplitude of voltage harmonics are the same, yielding the same THD_v. However, when moving from an *8MVAr* system to a *6 kVAr* system, the parameters of transformer, reactors, and switching devices change, impacting losses.

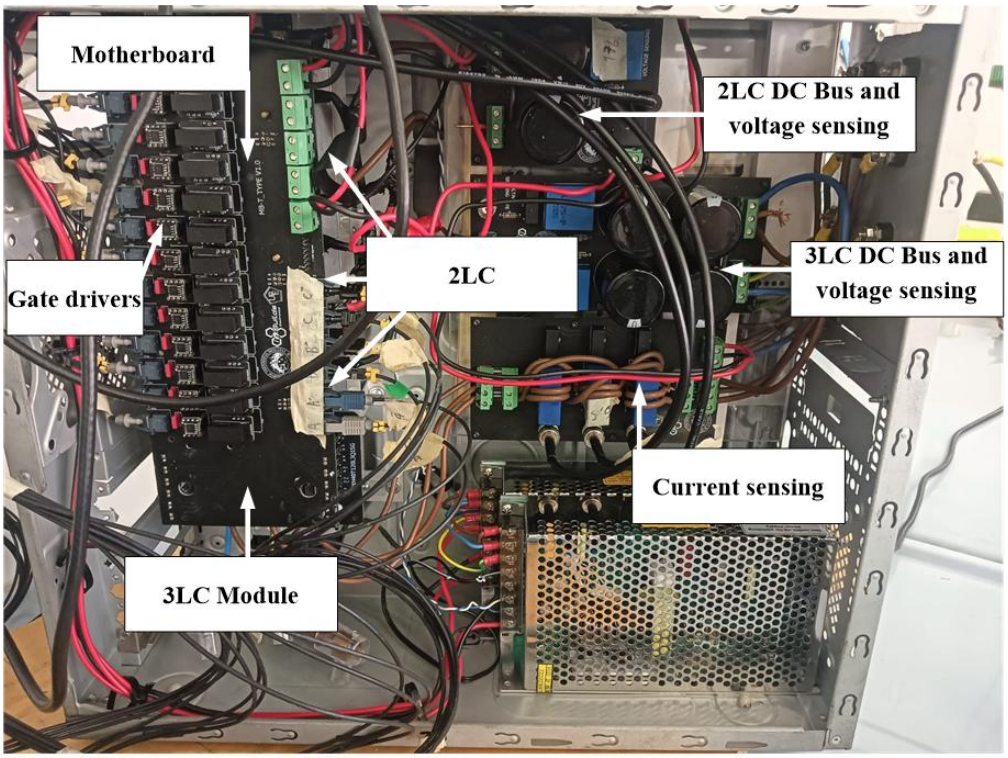


Fig. 6.14 6kVA Prototype.

Figures 6.15 and 6.16 deal with steady-state operations of the scaled-down prototype under balanced load conditions in both inductive and capacitive modes, with V_{DC2}=*150V*. Key quantities are shown, including the grid phase-voltage e_{jg}, 3LC voltage V_{3LCa}, transformer secondary phase voltage V_{MVa}, 3LC DC bus capacitors voltages V_{C1} and V_{C2}, 2LC DC link voltage V_{DC2}, and MV side phase currents i_{MVj}. In inductive mode the current THD_i is 0.57%, while the THD of V_{MVa} is 0.72%. The latter is close to that (0.7%) obtained in the simulation of the *8MVAr* system according to Table 6.7. In comparison the current THD_i is higher (0.55% instead of 0.45%) since the inductance of the *6kVA* transformer is lower (*0.38 mH*) than that of the *12MVA* transformer (*3.14 mH*). However, the THD_i is well within the limits established by the IEEE Std. 519-2014 standard.

Tab. 6.7 6kVar Scaled Converter parameters.

3LC	
Rated power	+-6kVar
DC bus voltage	540V
RMS line to line voltage at α=15°	400 V
DC Link Capacitors	2 x 1mF
Switching frequency	50Hz
SI-IGBT Module	FS3L30R07W2H3F_B11, 650V, 30A
Gate drivers	1EDI60N12AF
2LC	
Rated power	6kW
DC bus voltage	150V
RMS line to line voltage	100 V
Harmonics eliminated	$5^{th} \div 19^{th}$
DC Link Capacitor	1mF
Switching frequency	10kHz
SiC MOSFETs	SCT040HU65G3AG, 650V, 30A
Gate drivers	1EDI60N12AF
Coupling transformer	
Rated Power	6kVA
Rated Voltages	400V/400V
Total reactance	0.15Ω

Figure 6.17 illustrates the dynamic response of the system to a step variation of the reactive power from *2 kVar* to *4.5 kVar*. The capacitor voltages remain balanced during these transients. Figure 6.18 shows the response to a 3LC capacitors voltage imbalance generated by parallel connecting a *200 Ω* resistor to C_1. Despite the initial imbalance, the T-STATCOM was able to provide

sinusoidal currents as the 2LC effectively compensates for the unbalanced voltages. After *850ms*, the imbalance was corrected, restoring the correct capacitor voltages. Figure 6.19 deals with a *20%* symmetrical voltage sag of the grid voltage e_{jg}. The duration of the sag is *300ms*, during which the amplitude of the voltage at the POC, V_{HVj}, is kept constant, as well as the DC link voltage, V_{DC2}.

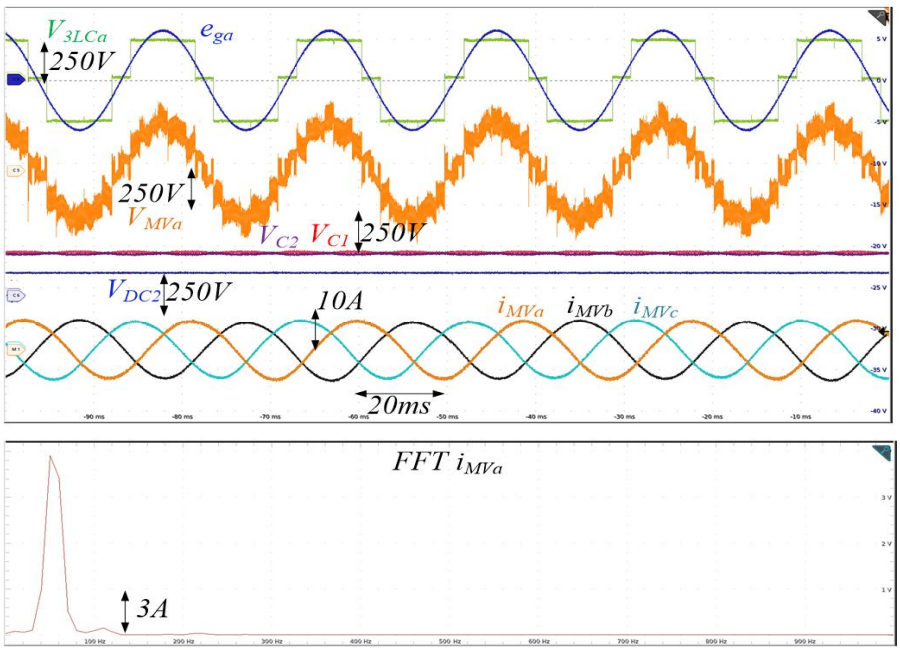


Fig. 6.15 Inductive mode: Balanced operation at +4.5kVAr, V_{DC1}=540V, V_{DC2}=150V, 10kHz.

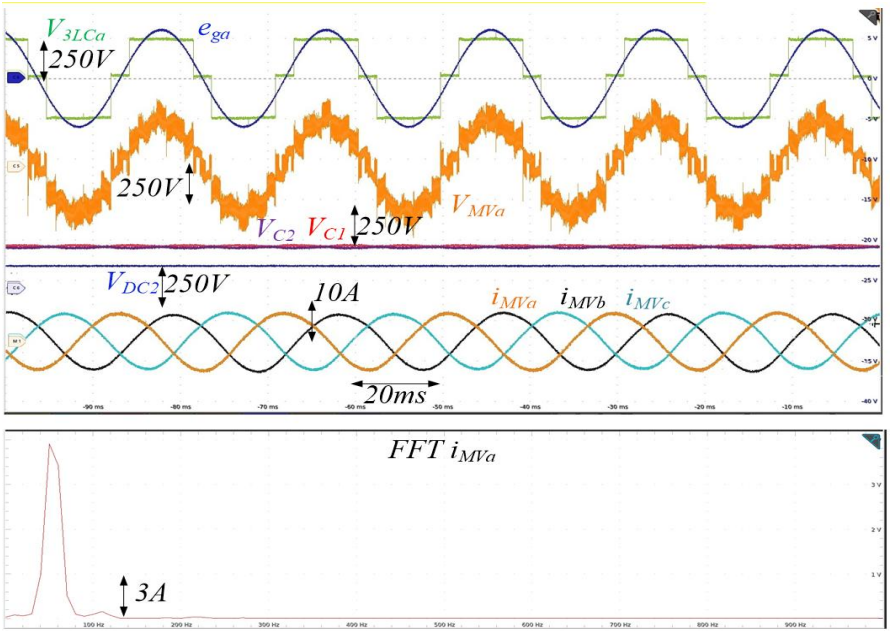


Fig. 6.16 Capacitive mode: Balanced operation at -4.5kVAr, V_{DC1}=540V, V_{DC2}=150V, 10kHz.

A 40% symmetrical voltage sag is considered in Fig. 6.20. An asymmetrical 20% voltage sag affecting only the *a*-phase is shown in Fig. 6.21. Within half a fundamental period, control is able to restore both the voltage and the current. The impact of a low voltage ratio k_v on power quality is illustrated in Fig. 6.22. When reducing k_v to *0.13* the 2LC is unable to fully compensate the full set of harmonics, and particularly the 5^{th} and 7^{th} become relevant. This causes a 6% THD_v and a 4.5% THD_i, exceeding the standard limits. A power quality analysis is presented in Table 6.8, which shows the amplitude of voltage and current harmonics at *10kHz* on the HV side (POC), for both capacitive and inductive cases. The THD_v results are similar to the simulated case at *8MVar*, while the THD_i values are higher because the inductance of the *6kVA* transformer is lower than that of the *12MVA* one.

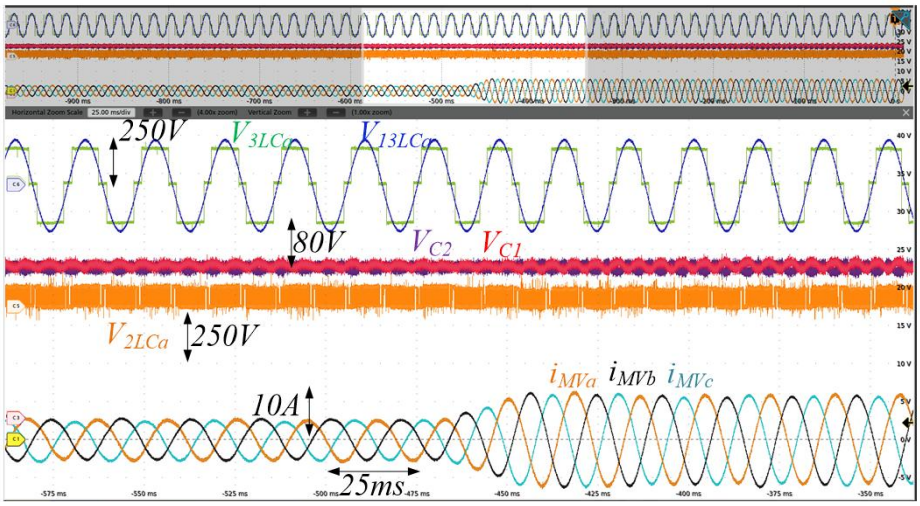


Fig. 6.17 Reactive power variation from 2kVAr to 4.5kVAr, V_{DC1}=540V, α=15°, V_{DC2}=150V, 10kHz.

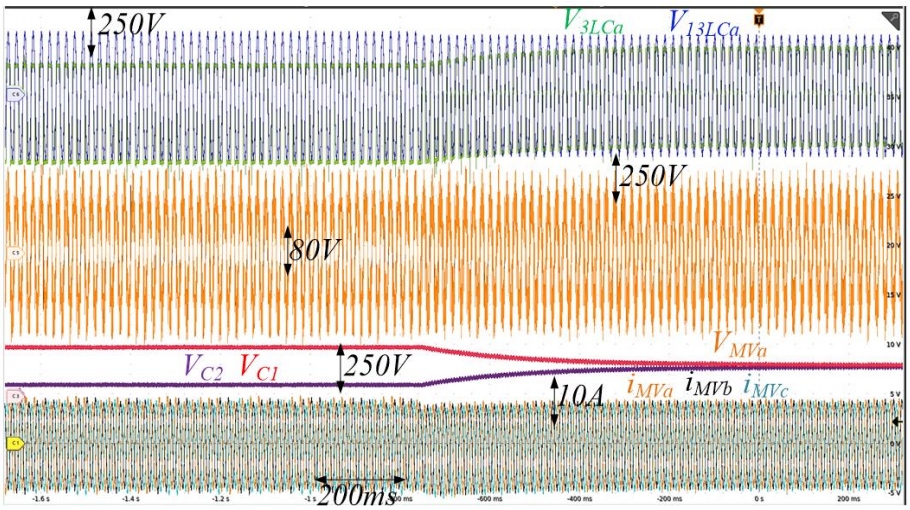


Fig. 6.18 DC bus capacitors voltage balancing, 4.5kVAr, V_{DC1}=540V, α=15°, V_{DC2}=150V, 10kHz.

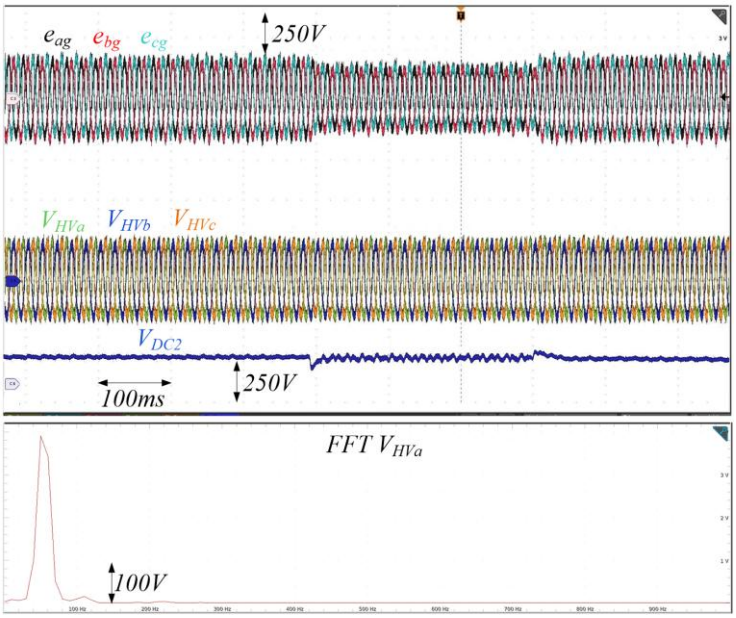


Fig. 6.19 Voltage regulation at the POC during 20% symmetrical grid voltage sag, k_v=0.27, V_{DC1}=540V, α=15°, V_{DC2}=150V, 10kHz.

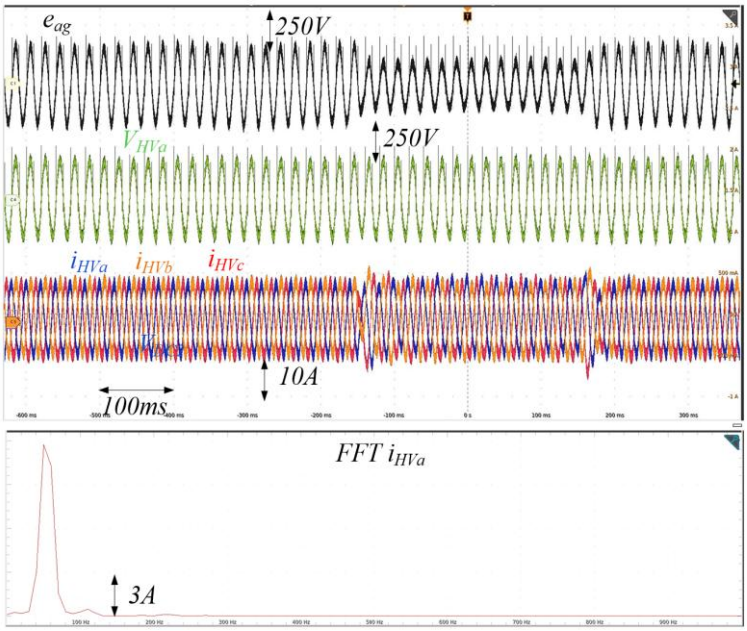


Fig. 6.20 Voltage regulation at the POC during 40% symmetrical grid voltage sag, k_v=0.27, V_{DC1}=540V, α=15°, V_{DC2}=150V, 10kHz.

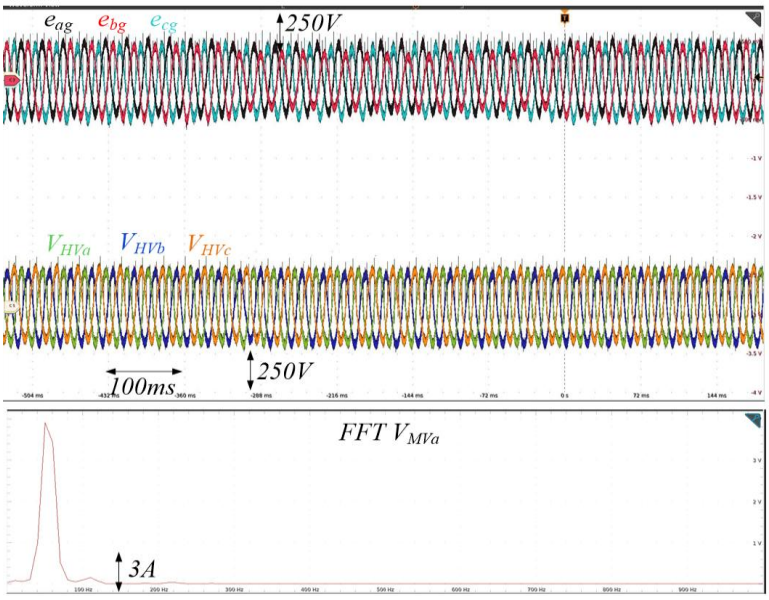


Fig. 6.21 Voltage regulation at the POC during an asymmetrical voltage sag caused by a 20% reduction in grid voltage on the a-phase, k_v=0.27, V_{DC1}=540V, α=15°, V_{DC2}=150V, 10kHz.

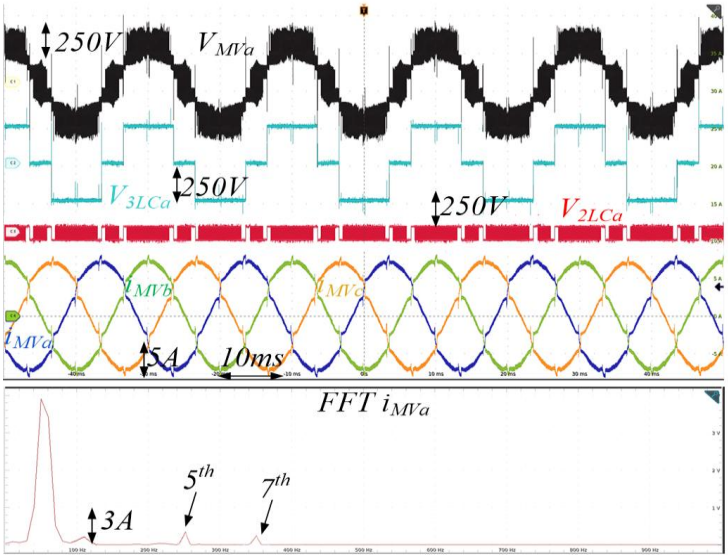


Fig. 6.22 Effect of a low voltage ratio k_v=0.13, 4.5kVAr, V_{DC1}=540V, α=15°, V_{DC2}=75V, 10kHz.

A power losses analysis was also accomplished. First, the total losses were measured versus the reactive power to compare them with results obtained by simulation of the scaled down converter. Accurate models of the switching devices, capacitors, and AC transformer have been used so that simulation results closely match measured losses, as shown in Fig. 6.23, with an error of less than 5%. The consistent correlation between experimental and simulation results makes possible to individually estimate by simulation switching and conduction losses, as shown in Fig. 6.24. The switching losses in the 3LC are almost negligible due to low-frequency modulation, while conduction losses are higher compared to the 2LC, which uses SiC-MOSFETs. Finally, the experimental results obtained from the tested *6kVAr* prototype demonstrate high reliability even when extrapolated to a potential *8MVAr* application. Indeed, the two-level converter operates as an active filter, mitigating voltage harmonics. Consequently, scaling up the power level primarily impacts the overall power losses, which will increase alongside the cost of the passive components. Nevertheless, the harmonic content remains unaffected by the overall power increase, ensuring that the filtering performance remains strictly constant.

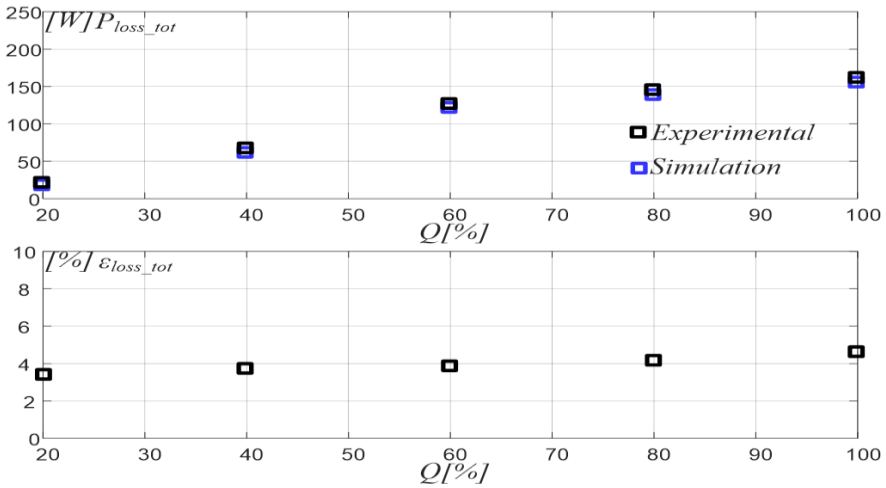


Fig. 6.23 Power losses: experimental and simulation results at 10kHz.

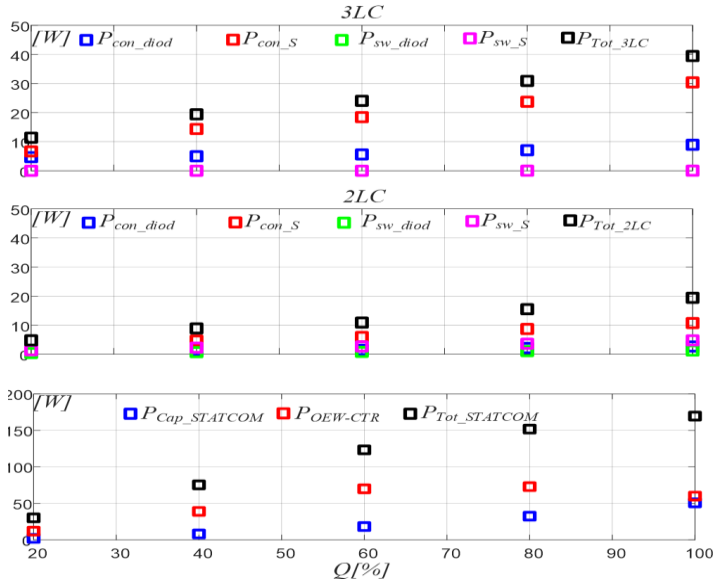


Fig. 6.24 Estimated power losses at 10kHz. From top: 3LC and 2LC conduction, switching and total power losses vs. reactive power. Capacitor, coupling transformer and total power losses.

Table 6.8 Voltage and current harmonics at the HV Side at ±4.5KVar, 10kHz.

Harmonic order	Inductive Q=4.5kVar		Capacitive Q=-4.5kVar	
	V_{HVa}(%)	i_{HVa} (%)	V_{HVa}(%)	i_{HVa} (%)
5th	0.3	0.15	0.22	0.11
7th	0.24	0.23	0.21	0.2
11th	0.19	0.29	0.35	0.29
13th	0.2	0.1	0.11	0.1
17th	0.36	0.16	0.24	0.2
19th	0.23	0.13	0.31	0.23
23rd	0.1	0.2	0.2	0.17
25th	0.14	0.14	0.2	0.14
29th	0.19	0.11	0.18	0.11
31st	0.14	0.1	0.21	0.14
35th	0.16	0.11	0.26	0.21
37th	0.13	0.11	0.3	0.21
41st	0.19	0.04	0.19	0.12
43rd	0.14	0.03	0.14	0.03
47th	0.16	0.02	0.16	0.12
49th	0.13	0.02	0.23	0.12
THD	0.72%	0.57%	0.9%	0.67%

6.6 COMPARATIVE ANALYSIS AND DISCUSSION.

PSIM simulation was used to compare in terms of component cost, losses and power quality the proposed topology with fourteen others possible STATCOM converter topologies, namely:

A. 5-Level CMC with Si-IGBTs switching at *10kHz.*
B. 5-Level CMC with SiC-MOSFETs switching at *10kHz*.
C. 5-Level NPC with Si-IGBTs switching at *10kHz*.
D. 5-Level NPC with SiC-MOSFETs switching at *10kHz*;
E. 11-Level CMC with Si-IGBTs switching at *10kHz.*
F. 11-Level CMC with SiC-MOSFETs switching at *10kHz*.
G. 19-Level AHMLC with Si-IGBTs switching at *50Hz* and SiC-MOSFETs switching at *15kHz* [22].
H. *23*-Level AHMLC with Si-IGBTs switching at *50Hz* and SiC-MOSFETs switching at *4.7kHz* [23].
I. *5*-Level NPC with Si-IGBTs switching at *0.9kHz* [7].
J. 5-Level NPC with Si-IGBTs switching at *8kHz* [5];
K. 11-Level CHB with Si-IGBTs switching at *0.5kHz* [14];
L. 17-Level CHB-NPC with Si-IGBTs switching at *1kHz* [19];
M. 21-Level MMC with Si-IGBTs switching at *1kHz* [11];
N. 21-Level MMC with SiC-MOSFETs switching at *1kHz* [11].

These topologies can be divided into three groups, namely, Si/WBG based topologies (G and H), fully Si-IGBT or SiC-MOSFET based 5-level topologies (A, B, C, D, I, J) and fully Si-IGBT based topologies featuring more than 5 levels (E, F, K, L, M and N). All STATCOM designs are rated at *8MVAr*. Some of the considered topologies have been developed for D-STATCOM applications, hence, they do not originally include a coupling transformer. However, for a fairy comparison, a step-up transformer has been introduced in these topologies to allow the connection to the *154kV* bus. Since the transformer increases the series reactance, the coupling reactor has been reduced accordingly to match the specifications reported in the referenced literature. The initial total cost of systems is estimated based on the actual market cost of switching devices, diodes, gate drivers, capacitors, reactors, and transformers. The transformer turns ratio t_r varies depending on the topology, while the power rating is constant. Based on data provided by Terna S.p.A., the

cost of the transformer does not vary significantly with the turns ratio, as it is primarily influenced by the rated power, which is held constant for all the considered topologies. Moreover, for a fair comparison, the total energy stored in the DC bus capacitors is set to *250kJ* on all the topologies. The number of capacitors required to store this energy is however variable, depending on the voltage level and capacitance value. Table 6.9 presents a comparison of the proposed topology with G and H ones. Topology G [20] encompasses *24 6.5kV* Si-IGBT modules, *30 1.2kV* Si-IGBT modules, and *6 1.2kV* SiC modules. It requires 32 capacitors and a *6mH* coupling reactor. Since the transformer inductance is *3.5mH*, an additional *2.5mH* reactor was connected in series. The higher number of power devices and the reactor makes the G topology approximately 77% more expensive than the proposed one. The topology H [21] requires *24 4.5kV* Si-IGBT modules and *12 1.2kV* SiC modules, *60* capacitors and a *20mH* reactor to reach the *22mH* design inductance. This results in a initial total cost approximately 160% higher than that of the proposed topology and *47%* higher compared to topology G. Table 6.10 deals with a comparison of the proposed topology with some CMC and NPC *5*-level topologies. The topology J has roughly the same component cost as the proposed topology, while the other topologies, are more expensive due to the higher number of power devices and the need for coupling reactors. Finally, in Tab. 6.11 the proposed topology is compared with *11*-level topologies (E, F, K), the *17*-level topology L, the *21*-level Si-IGBT based topology M and *21*-level SiC based N. The N topology is the most expensive, due to the high number of cells and the higher cost of *3.3 kV* SiC modules compared to the *3.3 kV* Si-IGBT modules used in topology M. Another kind of comparison was played in terms of power losses and voltage THD_v. Obtained results are listed in Table 6.12. The THD_v was computed in accordance with IEEE Std. 519-2014. All the considered topologies comply with the requirements of this standard (THD_v<*2.5%*) excepting topologies I and L. The proposed topology, thanks to the active harmonic cancellation achieves a 0.7% THD_v, comparable to that obtained by topologies E, F, H, G, L and M, which are equipped with coupling reactors.

Table 6.9a Characteristics comparison with topologies G and H.

Parameters		Rating	Unit cost	Proposed	G	H
Power				8 MVAr	8 MVAr	8 MVAr
Output voltage levels		\	\	6	19	23
Energy stored in the DC bus capacitors		\	\	250 kJ	250 kJ	250 kJ
V_{LLn}		\	\	8.3kV	6kV	6.6kV
Voltage stress	V_{CE} -SI-IGBT	\	\	5.5kV	0.7kV (CHB) 4kV (NPC)	2.3kV (Si-CHB)
	V_{DS} -SiC	\	\	3 kV	0.7 kV	0.65kV (SiC-CHB)

Table 6.9b Component cost comparison with topologies G and H.

Components	Rating	Unit cost	Proposed	G	H
SI-IGBT Module FZ750R65KE3	6.5kV, 750A	2,902 €	\	24	\
SI-IGBT Module FZ1000R65KE4	6.5kV, 1kA	3,161 €	12	\	\
SI-IGBT Module FZ1200R45KL3_B5	4.5kV, 1.2kA	2,113 €		\	24
SI-IGBT Module FZ1600R12HP4	1.2kV, 1.6kA	610 €	\	30	
SiC Module 726-FF1MR12MM1HWB11B	1.2kV, 1kA	810 €	\	\	12
SiC Module FF3MR20W3M1HH11BPSA1	1.2kV, 0.64kA H-Bridge	570 €	\	6	\
SiC Module FF2000UXTR33T2M1	3.3kV, 1kA H-Bridge	6441 €	3	\	\
Diode RBK86525XX-ND	6.5kV, 2.5kA	538 €	6	6	\
Capacitor ERHB701LGC102MDB5U	700V,4mF, ESR 17mΩ	235 €	\	26 CHB	36 SiC-CHB
Capacitor Electronicon MKP	2kV,4.6mF, ESR 17mΩ	480 €	20	6 NPC	24 Si-CHB
Gate driver 1SD536F2	/	339 €	18	60	48
Number of DC Bus	\	\	3	11	12
Three-Phase Transformer	12MVA, 154kV/9kV	150,000 €	1	1	1
Coupling Reactor	12MVAr, 12kV, 2,5mH	43,440 €	\	3	\
Coupling Reactor	12MVAr, 12kV, 20mH	114,000 €			3
Tot. Estimated Cost €			**226,190**	**401,000**	**588,700**

Table 6.10a Characteristics comparison with topologies I, J, A, B, C and D.

Parameters		**Ratings**	**Unit cost**	**Proposed**	**I**	**J**	**A**	**B**	**C**	**D**
Power				8 MVAr	8 MVAr	8 MVAr	8 MVAr	8 MVAr	8 MVAr	
N_L		\	\	6	5	5	5	5	5	5
Energy		\	\	250 kJ	250 kJ	250 kJ	250 kJ	250 kJ	250 kJ	250 kJ
V_{LLn}		\	\	8.3kV	8.3kV	8.3kV	8.3kV	7.4kV	8.3kV	8.3kV
Voltage stress	V_{CE} - SI-IGBT	\	\	5.5kV	2.7kV	4kV	3.3kV	3kV	2.75kV	2.75kV
	V_{DS} - SiC	\	\	3 kV	\	\	\	\	\	\

Table 6.10b Component cost comparison with topologies I, J, A, B, C and D.

Components	**Ratings**	**Unit cost**	**Proposed**	**I**	**J**	**A**	**B**	**C**	**D**
SI-IGBT Module FZ1000R65KE4	6.5kV, 1kA	3,161 €	12	\	\				
SI-IGBT Module FZ1200R45KL3_B5	4.5kV, 1.2kA	2,113 €		24	18	24		24	
SiC Module FF2000UXTR33T2M1	3.3kV, 1kA H-Bridge	6441 €	3	\	\		12		12
Diode RBK86525XX-ND	6.5kV, 2.5kA	538 €	6	\	\				
Diode IXYS E1250HC45E	4.5 kV, 1.7kA	997 €						18	18
Capacitor Electronicon MKP	2kV, 4.6mF, ESR 17mΩ	480 €	20	60	63	38	38	56	56
Gate drive 1SD536F2	/	339 €	18	24	18	24	24	24	24
Number of DC Bus			3	6	3	6	6	4	4
Three-Phase Transformer	12MVA, 154kV/9kV	150,000 €	1	1	1	1	1	1	1
Coupling Reactor	12MVAr 12kV, 2,5mH, Rs=0.12Ω	43,440 €	\	3	\	3	3	3	3
Tot. Estimated Cost €			**226,200**	**368,000**	**224,300**	**357,400**	**384,000**	**384,000**	**410,500**

Configuration H achieves the lowest THD_v (0.47%). Power losses were estimated using precise models developed on the joint Simulink and PSIM simulation platform. Table 6.12 deals with conduction and switching losses in the power switches and diodes, as well as with losses in the capacitors, transformer and coupling reactors. The proposed topology achieves the lowest total power loss (2%). The proposed topology provides the best balance of cost, THD_v and power losses of all the considered topologies. It has a initial total cost of around *€226,000* and very low total losses, with a THD_v below 2.5%. This is thanks to the use of SiC-MOSFETs, which significantly reduce switching losses, and line frequency commutation of Si-IGBTs. The component cost issue posed by a converter based entirely on SiC-MOSFETs is resolved by combining SiC-MOSFETs with less expensive Si-IGBTs in a way that exploits the best features of both types of devices, using an open-end winding configuration. This allows Si-IGBT modules to be commutated at line frequency, minimizing switching power losses, while SiC-MOSFETs operate in PWM mode to precisely shape voltages and currents with high efficiency. Furthermore, SiC-MOSFETs are commutated at the minimum possible frequency (*10÷15kHz*), enabling the cancellation of voltage harmonics up to the 19^{th} order to further improve efficiency. Being more efficient the proposed T-STATCOM configuration produces significantly less heat than conventional configurations that rely entirely on traditional Si-IGBTs, or that include passive components like reactors. Therefore, the proposed structure requires smaller and less expensive cooling systems, taking also advantage of the high operating temperature of SiC-MOSFETs. Due to their critical role in reactive power regulation and overall system stability, protection measures that ensure operational reliability during grid fault conditions are essential in STATCOMs. Fault ride-through capability is achieved through current-limiting control strategies, which enable reactive current injection to remain within safe thermal margins even in the event of short circuits or voltage sags. In the proposed topology, thermal tolerance is further enhanced by combining SiC-MOSFETs, which can operate at high temperatures, with low-frequency commutated Si-IGBTs, which are able of sustaining higher currents than PWM-operated devices due to their negligible switching losses. In the event of a converter failure, the OEW configuration of the proposed topology enables the star point of the transformer winding connected to the faulty side to be closed, allowing the system to operate at reduced power using the healthy inverter. In all cases, the fault management techniques established in conventional STATCOMs can be adapted to this specific configuration. The switching of SiC-MOSFETs at high voltages and frequencies can lead to electromagnetic compatibility (EMC) issues,

primarily due to the high $\frac{dv}{dt}$ levels. In this regard, the proposed topology offers an advantage over fully SiC-MOSFET-based topologies, as it mitigates these issues through the reduced number of SiC devices employed, the lower switching frequency, leading to a reduced number of switching events per second, and the lower commutated voltage. Furthermore, the CMV does not pose a concern, since the transformer at the inverter output provides effective isolation against CMC [26]. Table 6.13 summarizes both simulation and experimental results for the proposed reactive power compensation system, evaluated at a switching frequency of *10kHz* and a voltage ratio k_v of *0.27*. Simulation results, conducted on an 8MVar system, indicate a THD_v of 0.7% during inductive operation and 0.87% during capacitive operation, with corresponding power losses of 2%. Experimental validation on a *6kVar* system shows comparable performance, with THD_v values of 0.72% and 0.9% for inductive and capacitive operation, respectively, and slightly higher power losses of 2.6%. A comparison with multi-level converter topologies highlights the advantages of the proposed system. Relative to a 5-level converter, the proposed design reduces power losses by 20% at a marginal component cost increase of 0.9%, while decreasing THD_v by 27%. Compared to an 11-level converter, power losses are halved (50% reduction), and component cost is reduced by 45%, albeit with a 30% increase in THD_v. For systems exceeding 17 levels, power losses decrease by 45%, costs drop by 50%, but THD_v increases by *32%.*

Table 6.11a: Characteristics comparison with topologies K, E, F, L, M and N.

Parameters		**Rating**	**Unit cost**	**Proposed**	**K**	**E**	**F**	**L**	**M**	**N**
Power				8 MVAr	8 MVAr	8 MVAr	8 MVAr	8 MVAr	8 MVAr	8 MVAr
N_L		\	\	6	11	11	11	17	21	21
Energy		\	\	250 kJ	250 kJ	250 kJ	250 kJ	250 kJ	250 kJ	250 kJ
V_{LLn}		\	\	8.3kV	10.5kV	11kV	11kV	10kV	25kV	25kV
Voltage stress	V_{CE} Si-IGBT	\	\	5.5kV	1.8kV	2.2 kV	2.2 kV	1.25kV(NPC) 2.5kV(CHB)	3.3 kV	\
	V_{DS} SiC	\	\	3 kV	\	\	\	\	\	3.3 kV

Table 6.11b: Component cost comparison with topologies K, E, F, L, M and N.

Components	Ratings	Unit cost	Proposed	K	E	F	L	M	N
SI-IGBT Module FZ1000R65KE4	6.5kV, 1kA	3,161 €	12	\	\	\	\	\	
SI-IGBT Module FZ800R45KL3_B5	4.5kV, 0.8kA	1,600 €	\	\	\	\	36	\	
SI-IGBT Module FZ1200R33HE4DB9BPSA1	3.3kV, 1.2kA	1,500 €	\	60	60	\	\	\	
SI-IGBT Module FF450R33T3E3	3.3kV, 0.45kA	1,332 €	\			\		66	
SI-IGBT Module FZ1200R17HP4_B2	1.7kV, 1.2kA	939 €	\	\			24	\	
SiC Module 726-FF1MR12MM1HWB11B	1.2kV, 1kA	810 €	\	\			\	\	
SiC Module FF2000UXTR33T2M1	3.3kV, 1kA	6441 €	3	\		30	\	\	66
Diode RBK86525XX-ND	6.5kV, 2.5kA	538 €	6	\			\	\	
Diode IXYS E1250HC45E	4.5 kV, 1.7kA	997 €						\	
Diode DZ800S17K3	1.7kV, 0.8kA	134 €	\	\			12	\	
Capacitor Electronicon MKP	2kV, 4.6mF, 17mΩ	480 €	20	30	90	90	120	30	30
Gate driver 1SD536F2	/	339 €	18	60	60	60	72	132	132
Number of DC Bus			3	15	15	15	15	66	66
Coupling Trans.	12MVA, 54kV/9kV	150,000€	1	1	1	1	1	1	1
Coupling Reactor	2,5mH 12MVAr 12kV	43,400€	\	3	3	3	3	6	6
Tot. Estimated Cost €			**226,000**	**405,000**	**434,000**	**537,000**	**444,000**	**558,000**	**840,000**

Table 6.12 Power Losses and THD_v Comparison.

		A	**B**	**C**	**D**	**J**	**I**	**E**	**F**	**K**	**L**	**H**	**G**	**M**	**N**	**Proposed**
THD_v [%]		1	1.5	1.4	1.4	0.9	3.4	0.5	0.6	1.5	13	0.5	0.5	0.5	0.5	0.7
N_L		5	5	5	5	5	5	11	11	11	17	23	19	21	21	6
f_{sw} [kHz]		10	10	10	10	8	0.9	10	10	0.5	1	4.7	15	1	1	10
P_{Cond} [%]	Si	1.1	\	1	\	0.2	1.1	1.5	\	1.9	2.2	0.8	0.5	1.5		0.5
	SiC	\	0.9	\	0.7	\	\	\	1.2	\	\	0.3	0.3	\	1	0.3
P_{SW} [%]	Si	3.9	\	2.2	\	2.9	0.4	6.8	\	0.4	0.5	0.1	0.1	1.8	\	0.1
	SiC	\	1.7	\	0.9	\	\	\	1.5	\	\	0.2	0.1	\	0.3	0.2
Capacitor Losses [%]		0.1	0.1	0.1	0.1	0.1	0.1	0.2	0.2	0.1	0.3	0.2	0.1	0.1	0.1	0.1
Transformer Losses [%]		0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.6	0.6	0.8
Reactor Losses [%]		1.4	1.7	1.4	1.4	\	\	1.4	1.4	0.9	1	1.6	2.7	0.7	0.7	\
Total Losses [%]		**7.3**	**5.3**	**5.5**	**4**	**4.1**	**2.5**	**10.7**	**5.1**	**4.1**	**4.8**	**3.7**	**4.4**	**4.7**	**2.7**	**2**

In all cases, the THD_v remains well within the limits prescribed by the IEEE Std. 519-2014, ensuring compliance with industry harmonic requirements. Overall, these results demonstrate that the proposed configuration offers a favorable trade-off between efficiency, harmonic performance, and component cost compared to conventional multi-level configurations. Experimental results corroborate the simulation trends, confirming the robustness of the design under both inductive and capacitive operating conditions. Investigation on additional features, such as life cycle costs and reliability, could provide a basis for future works. Specifically, while the cost analysis highlighted the economic advantage of the proposed solution, it must be noted that installation, maintenance, and lifecycle costs were not considered due to the difficulty in obtaining reliable data for all configurations. Nevertheless, some qualitative considerations can be drawn regarding these

aspects for the evaluated STATCOM topologies. Topologies with a high number of levels require a significant number of components and bulky sub-module capacitors, which inevitably increases the overall system footprint and weight. They also generally facilitate maintenance operations due to their inherent modularity, allowing for quick replacement of faulty sub-modules and the implementation of fault-tolerant control strategies. Furthermore, AHMLC, utilizing an open-end winding configuration, present unique installation challenges. This setup mandates physical access to both ends of the transformer windings, leading to increased cabling complexity, higher insulation requirements, and the need for a customized transformer design but hybrid solutions combining increase the complexity of the hardware control and gate drive circuitry, potentially requiring more specialized diagnostic and maintenance procedures. Finally, the operational lifespan of these systems is heavily influenced by their component count and thermal stress. The extensive use of WBG can mitigate thermal cycling fatigue, potentially extending the power devices' lifecycle. Conversely, topologies relying on a massive number of active switches statistically face a lower Mean time between failures. To ensure a long lifecycle in highly multilevel configurations, the inclusion of redundant modules is strictly necessary, which in turn feeds back into higher initial capital costs.

Table 6.13 Summary of Results.

Simulation results on 8MVar at 10kHz, k_v=0.27			
0.7% THD_v Inductive mode	0.87% THD_v Capacitive mode		2% Power losses
Comparison			
Compared to	**Power losses**	**Component cost**	**THD_v**
5-Level	20% reduction	0.9% higher	27% reduction
11-Level	50% reduction	45% reduction	30% higher
>17-Level	45% reduction	50% reduction	32% higher
Experimental results on 6kVar at 10kHz, k_v=0.27			
0.72% THD_v Inductive mode	0.9% THD_v Capacitive mode		2.6% Power losses

6.7 CONCLUSIONS.

A T-STATCOM converter topology featuring a coupling transformer with an open secondary winding has been proposed, combining a three-level NPC inverter using Si-IGBTs with a two-level inverter using SiC-MOSFETs. This hybrid approach exploits the advantages of both devices: very low switching losses are achieved by

operating the Si-IGBTs at line frequency, while the SiC-MOSFETs, switched in PWM mode at *10kHz*, accurately shape the output voltage and current and actively cancel significant harmonics. This eliminates the need for bulky passive filters, reducing both initial system cost and size while improving overall efficiency. Simulation results on an *8MVar* system show THD_v of 0.7% in inductive mode and 0.87% in capacitive operation with 2% power losses, while experimental tests on a *6kVar* prototype confirm similar performance, with THD_v of 0.72% and 0.9% and slightly higher losses of 2.6%. On average, the proposed system reduces both component cost and power losses by 20-50% compared to conventional MLCs, while keeping THD_v within the limits of IEEE Std. 519-2014. Future research will focus on life-cycle cost and reliability analysis, as well as the integration of GaN devices into STATCOM systems. The achievable power levels will depend on the advancement of GaN technology in terms of voltage and current ratings. The fast-switching capabilities and low losses of GaN devices are expected to further enhance system efficiency and reduce the physical size of STATCOM units, enabling more compact, high-performance reactive power compensation solutions.

6.8 REFERENCE LIST.

[1] Renewable Development and Connection Activities. Terna. (2023), www.terna.it;

[2] Kumar, Amit, Milad Moradpour, Michele Losito, Wulf-Toke Franke, Suganthi Ramasamy, Roberto Baccoli, and Gianluca Gatto. 2022. "Wide Band Gap Devices and Their Application in Power Electronics" *Energies* 15, no. 23: 9172. https://doi.org/10.3390/en15239172;

[3] S. Sharma *et al*., "A Comprehensive Review on STATCOM: Paradigm of Modeling, Control, Stability, Optimal Location, Integration, Application, and Installation," in *IEEE Access*, vol. 12, pp. 2701-2729, 2024, doi: 10.1109/ACCESS.2023.3345216;

[4] S.P. Gawande, M.R. Ramteke, “Three-level NPC inverter based new DSTATCOM topologies and their performance evaluation for load compensation”, International Journal of Electrical Power & Energy Systems, Volume 61,2014, Pages 576-584, ISSN 0142-0615, https://doi.org/10.1016/j.ijepes.2014.03.065;

[5] B. Gultekin and M. Ermis, "Cascaded Multilevel Converter-Based Transmission STATCOM: System Design Methodology and Development of a 12 kV ±12 MVAr Power Stage," in *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4930-4950, Nov. 2013, doi: 10.1109/TPEL.2013.2238642;

[6] Noman, Abdullah M. 2025. "A Novel Modified Delta-Connected CHB Multilevel Inverter with Improved Line–Line Voltage Levels" *Electronics* 14, no. 9: 1711. https://doi.org/10.3390/electronics14091711;

[7] L. Adam, T. Komrska, F. Iška and Z. Peroutka, "Maximizing Output Voltage of Three-Phase Nine-Leg Multilevel STATCOM by Minimum Infinity Norm Optimization," in IEEE Transactions on Industrial Electronics, vol. 72, no. 9, pp. 8747-8756, Sept. 2025, doi: 10.1109/TIE.2025.3546342;

[8] Choudhury, Subhashree, Mohit Bajaj, Taraprasanna Dash, Salah Kamel, and Francisco Jurado. 2021. "Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects" *Energies* 14, no. 18: 5773. https://doi.org/10.3390/en14185773;

[9] R. O. d. Sousa, A. F. Cupertino, L. M. F. Morais, H. A. Pereira and R. Teodorescu, "Experimental Validation and Reliability Analyses of Minimum Voltage Control in Modular Multilevel Converter-Based STATCOM," in *IEEE Transactions on Industrial Electronics*, vol. 71, no. 7, pp. 6546-6555, July 2024, doi: 10.1109/TIE.2023.3303634.

[10] H. Mohammadi P. and M. T. Bina, "A Transformerless Medium-Voltage STATCOM Topology Based on Extended Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1534-1545, May 2011, doi: 10.1109/TPEL.2010.2085088;

[11] Y. Yang and I. Colak, "Performance Comparison of Si and SiC Semiconductor Based Modular Multilevel Converters for Medium Voltage STATCOM," *2020 IEEE 61th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, Riga, Latvia, 2020, pp. 1-5, doi: 10.1109/RTUCON51174.2020.9316572;

[12] K. Fujii, U. Schwarzer and R. W. De Doncker, "Comparison of Hard-Switched Multi-Level Inverter Topologies for STATCOM by Loss-Implemented Simulation and Cost

Estimation," *2005 IEEE 36th Power Electronics Specialists Conference*, Dresden, Germany, 2005, pp. 340-346, doi: 10.1109/PESC.2005.1581646;

[13] S. Du, J. Liu, J. Lin and Y. He, "A Novel DC Voltage Control Method for STATCOM Based on Hybrid Multilevel H-Bridge Converter," in *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 101-111, Jan. 2013, doi: 10.1109/TPEL.2012.2195508;

[14] B. Gültekin *et al*., "Design and implementation of a 154 kV, ±50 MVAr Transmission STATCOM based on 21-level Cascaded Multilevel Converter," *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, USA, 2010, pp. 3936-3948, doi: 10.1109/ECCE.2010.5617795;

[15] H. H. Khan, G. Courteau, S. Kissling, A. Testa, S. Foti and M. Carpita, "Assessment of the Star Connected Cascaded H-Bridge to be used in STATCOM application," *2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Napoli, Italy, 2024, pp. 1136-1146, doi: 10.1109/SPEEDAM61530.2024.10609213;

[16] Priya, M., Ponnambalam, P. and Muralikumar, K. (2019), Modular-multilevel converter topologies and applications – a review. IET Power Electronics, 12: 170-183. https://doi.org/10.1049/iet-pel.2018.5301;

[17] K. Sano and M. Takasaki, "A Transformerless D-STATCOM Based on a Multivoltage Cascade Converter Requiring No DC Sources," in *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2783-2795, June 2012, doi: 10.1109/TPEL.2011.2174383;

[18] I. Jahn, C. D. Townsend and H. Z. de la Parra, "Model-predictive modulation strategy for a hybrid Si-SiC cascaded H-bridge multi-level converter," *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, Germany, 2016, pp. 1-10, doi: 10.1109/EPE.2016.7695434;

[19] Miremad, A., Monfared, K. K., Iman-Eini, H., & Neyshabouri, Y. (2020). Design and control of a STATCOM based on hybrid cascaded H-bridge and full-bridge neutral point clamped multilevel inverter. IET Power Electronics, 13(17), 4019-4030. https://doi.org/10.1049/iet-pel.2020.0726;

[20] X. Liu, J. Lv, C. Gao, Z. Chen and S. Chen, "A Novel STATCOM Based on Diode-Clamped Modular Multilevel Converters," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 5964-5977, Aug. 2017, doi: 10.1109/TPEL.2016.2616495;

[21] Foti, Salvatore, Antonio Testa, Salvatore De Caro, Luigi Danilo Tornello, Giacomo Scelba, and Mario Cacciato. 2021. "Multi-Level Multi-Input Converter for Hybrid Renewable Energy Generators" *Energies* 14, no. 6: 1764. https://doi.org/10.3390/en14061764;

[22] Y. Hou, Q. Guo, P. Ren, C. Tu, Z. Huang and W. Jia, "A Hybrid Cascaded Multilevel Converter Based on Si and SiC Devices and Its Regulation Optimization Strategy," in *IEEE Transactions on Industry Applications*, vol. 60, no. 3, pp. 4001-4011, May-June 2024, doi: 10.1109/TIA.2024.3355029M;

[23] Y. Koyama, Y. Nakazawa, H. Mochikawa, A. Kuzumaki, K. Sano and N. Okada, "A Transformerless 6.6-kV STATCOM Based on a Hybrid Cascade Multilevel Converter Using SiC Devices," in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7411-7423, Sept. 2018, doi: 10.1109/TPEL.2017.2770143;

[24] L. Maharjan, T. Tajyuta, K. Maruyama, A. Suzuki and A. Toba, "Development and Verification Test of the 6.6-kV 200-kVA Transformerless SDBC-Based STATCOM Using

SiC-MOSFET Modules," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13687-13696, Dec. 2020, doi: 10.1109/TPEL.2020.2995159;

[25] Cao, Yijia, Jiaqi Yu, Yong Xu, Yong Li, and Jingrong Yu. 2017. "An Efficient Phase-Locked Loop for Distorted Three-Phase Systems" *Energies* 10, no. 3: 280. https://doi.org/10.3390/en10030280;

[26] S. Shabani , M. Asadi , A. Zakipour, " Modeling and Simulation of Common Mode Voltage in a Three-Phase Delta Connection STATCOM with Parasitic Capacitors," in Iranian Journal of Electrical and Electronic Engineering, Vol. 19, no. 1, pp. 1-9, Mar. 2023.

CHAPTER 7

Conclusions.

7 CONCLUSIONS.

7.1 FUTURE WORKS

Looking ahead, the future trajectory of this research is intrinsically linked to the evolving technological and economic landscape of semiconductor materials. While WBG devices like SiC and GaN offer undeniable high-frequency and thermal advantages, their integration remains technologically demanding, and their future economic competitiveness against highly mature Si technology is not guaranteed. Current market dynamics indicate that the complex, defect-prone manufacturing processes of WBG wafers continue to sustain a significant price premium, making a wholesale transition to full-WBG systems economically prohibitive for many mass-market applications. Consequently, the hybrid Si/WBG topologies proposed in this thesis represent a robust, long-term design paradigm rather than a mere transitional compromise.

Future research must aggressively address the physical integration challenges inherent in these asymmetric architectures, particularly the management of severe EMI induced by disparate switching transients and the development of heterogeneous thermal management systems capable of handling localized WBG hotspots without degrading adjacent Si components.

In the realm of electric vehicles, while full-SiC drivetrains are currently penetrating the premium automotive sector, future developments of the proposed hybrid converters hold the key to enabling highly efficient architectures for mass-market vehicles. Research in this domain will likely pivot toward integrating these dual-inverter setups directly into motor housings, optimizing partial-load efficiency through dynamic modulation strategies that perfectly match standard urban driving cycles.

Concurrently, in the renewable energy generation sector, future implementations will focus on scaling these open-end winding topologies to multi-megawatt wind and utility-scale solar installations. By leveraging WBG devices as active, high-frequency harmonic compensators, future hybrid converters could drastically reduce the physical footprint and cost of passive LCL grid filters, utilizing predictive digital algorithms that adjust the power-sharing ratio between Si and WBG stages in real-time based on fluctuating environmental conditions.

Finally, grid-level power electronics, specifically FACTS such as STATCOMs, represent a highly demanding yet promising frontier for hybrid architectures. As

modern smart grids become increasingly saturated with non-linear loads and distributed energy resources, bulk reactive power must be managed reliably. Future hybrid FACTS devices will allow ultra-reliable, high-voltage Silicon components to handle the fundamental grid flows, while modular WBG active filters cleanly mitigate high-frequency harmonics, ensuring grid stability and power quality without the astronomical infrastructure costs associated with multi-megawatt full-SiC implementations.

7.2 CONCLUSIONS.

In conclusion, this doctoral research has addressed the critical challenge of balancing performance and cost in modern power electronics, demonstrating the overall effectiveness of hybrid semiconductor integration in advanced system design. By synergizing the maturity and cost-effectiveness of Si-IGBTs with the superior switching performance of WBG devices, the proposed architecture effectively bridges the gap between traditional technologies and future all-WBG solutions.

In the domain of wind power generation, the implementation of a hybrid Si/GaN OEW configuration demonstrated the topology's capability to outperform competing solutions. As evidenced by the developed three-port conversion system, the hybrid approach achieved significant efficiency improvements compared to classic alternatives. Furthermore, the multi-level nature of the topology reduced CMV and THD, directly mitigating insulation stress on generators.

For the automotive sector, this research addressed the voltage rating limitations of current GaN technology. The proposed hybrid multilevel inverter validated the feasibility of using commercial *650V* GaN devices within *800V–1000V* EV powertrains. Experimental validation highlighted a substantial reduction in THDv compared to traditional structures, leading to superior waveform quality and reduced torque ripple. Crucially, this performance was achieved with a system cost comparable to standard solutions, proving that hybrid topologies can unlock high-efficiency electric mobility today without waiting for high-voltage GaN cost parity.

Finally, regarding grid infrastructure, the hybrid Si/WBG T-STATCOM topology proved that active harmonic cancellation can eliminate the need for bulky passive filters. The experimental results confirmed that the hybrid combination could reduce both component cost and power losses compared to conventional Multi-Level Converters, while maintaining a THD well within IEEE Std. 519-2014 limits. This underscores the potential for more compact and reliable reactive power compensation units. Tab. 7.1 presents the main results obtained in this thesis work. In particular, Tab. 7.1a shows results of Chapter 4, Tab. 7.1b shows results of Chapter 5 and Tab. 7.1c shows results of Chapter 6.

Table 7.1a Main results of Chapter 4.

Hybrid OEW converter for wind generators						
Topology	**Peak value of cycle efficiency and THDv (100%f)**					
	100% Load		**50% Load**		**25% Load**	
	η [%]	**THDv [%]**	**η [%]**	**THDv [%]**	**η [%]**	**THDv [%]**
C-DC-Bus	76.8	19.5	79.6	19.8	78.8	20.5
C-AC-Link	69.2	19.3	72	19.5	71.6	20.3
Dual-Grid Inv	64.4	18.9	67.6	18.9	67.6	19.9
3L-OEW-Gen	67.2	9.9	70.8	9.9	68.8	10.9
Proposed OEW	**81.6**	**4.4**	**86**	**5.3**	**86.2**	**6**

Table 7.1b Main results of Chapter 5.

Hybrid OEW inverter for electric vehicles					
Topology	Peak value of cycle efficiency and THDv (100%f)				
	100% Load		50% Load		Cost [€]
	η [%]	THDv [%]	η [%]	THDv [%]	
A	90.7	23.2	90.5	22.2	164
B	95.5	21	94.9	21.8	223
C	96.2	13	95.8	10.3	329
D	99	13.2	98.9	10.3	877
E	96	13.1	95.6	10.2	318
F	98.7	13.3	98.5	10.4	465
G	99.1	13.2	98.9	10.2	624
H	99.1	13.3	98.9	10.1	707
I	98.3	6.3	98	7	505
L	**99**	**6.2**	**98.9**	**7**	**645**

Table 7.1b Main results of Chapter 6.

Hybrid Si/WBG OEW converter for FACTS					
Topology	**f_{sw} [kHz]**	**N_L**	**THDv [%]**	**Losses [%]**	**Cost [€]**
A	10	5	1	7.3	357,400
B	10	5	1.5	5.3	384,000
C	10	5	1.4	5.5	384,000
D	10	5	1.4	4	410,500
E	10	11	0.5	10.7	434,000
F	10	11	0.6	5.1	537,000
G	15	19	0.5	4.4	401,000
H	4.7	23	0.5	3.7	588,700
I	0.9	5	3.4	2.5	368,000
J	8	5	0.9	4.1	224,300
K	0.5	11	1.5	4.1	405,000
L	1	17	13	4.8	444,000
M	1	21	0.5	4.7	558,000
N	1	21	0.5	2.7	840,000
Proposed	**10**	**6**	**0.7**	**2**	**226,000**
Compared to 5-Level			**27% lower**	**20% lower**	**0.9% higher**
Compared to 11-Level			**30% higher**	**50% lower**	**45% lower**
Compared to >17-Level			**32% higher**	**45% lower**	**50% lower**

In the final analysis, this work confirms that hybrid integration represents the most sustainable design pathway for modern power converters. Thanks to the strengths of Si, SiC, and GaN, the presented topologies transcend the performance limitations of silicon-only systems, delivering enhanced efficiency and compactness while maintaining a competitive cost structure. Furthermore, as vertical GaN structures and higher-rated WBG technologies continue to mature, these hybrid topologies provide a scalable, resilient, and immediate pathway for the advancement of next-generation power converters for renewable energy sources, electric vehicles and grid integration.